



Q67/ Q65/ H67/ H61 H2-AD

Rev : 1.0

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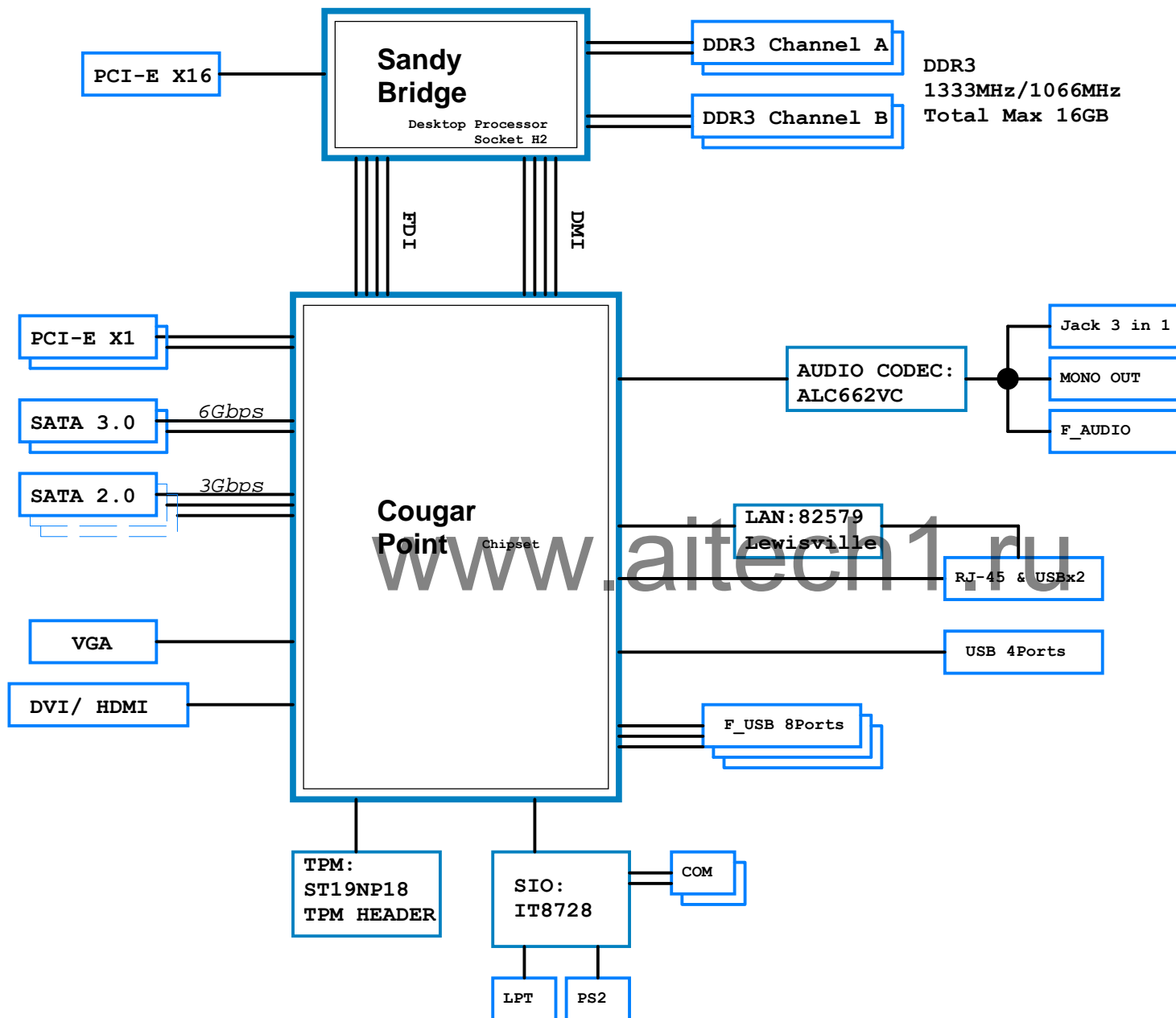
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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	



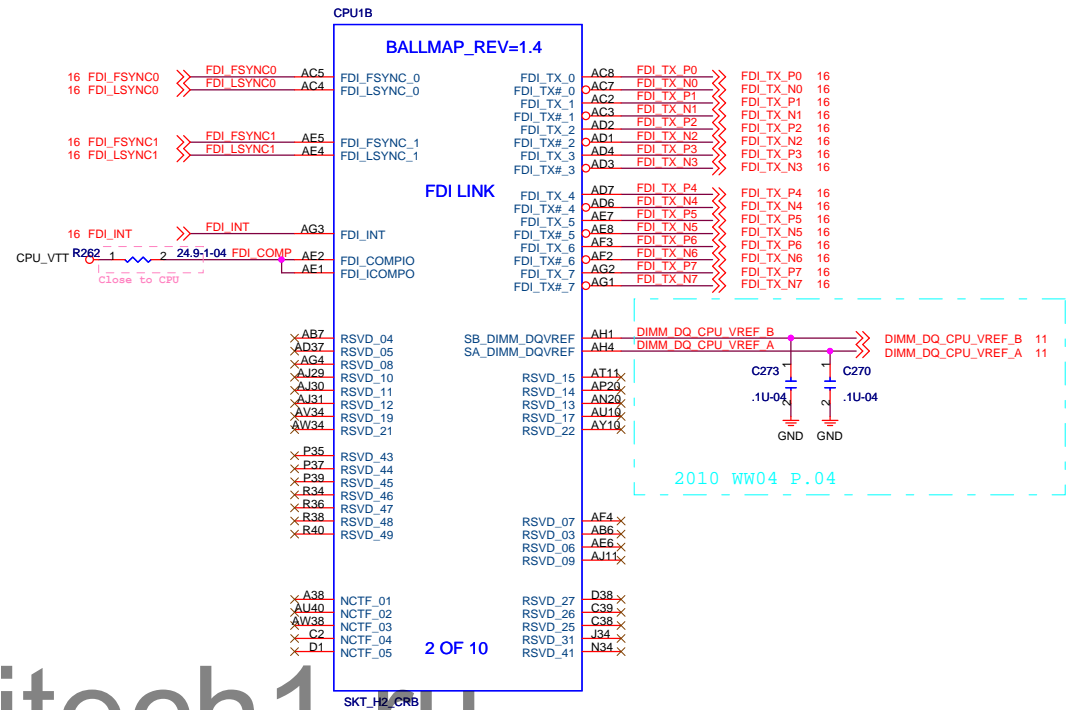
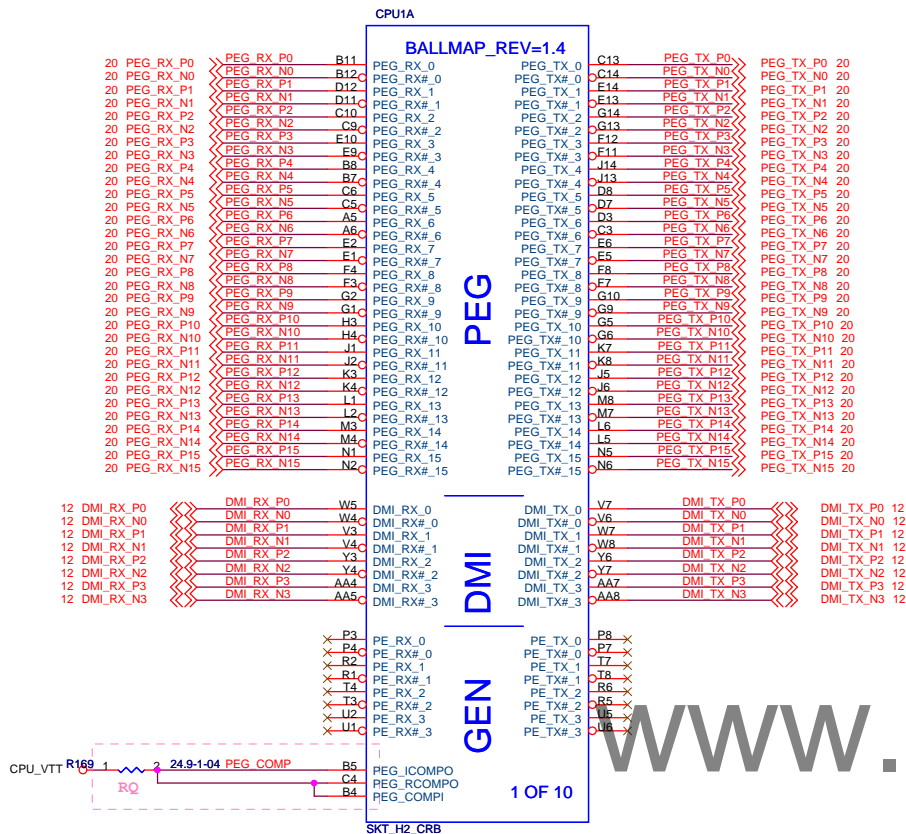
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A_L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A_P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A_N[0..3]
9 M_WE_A_L	← M_WE A_L
9 M_CAS_A_L	← M_CAS A_L
9 M_RAS_A_L	← M_RAS A_L

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B_L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B_P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B_N[0..3]
10 M_WE_B_L	← M_WE B_L
10 M_CAS_B_L	← M_CAS B_L
10 M_RAS_B_L	← M_RAS B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AL1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AN1	SA_DQ_7
M_DATA_A8	AN4	SA_DQ_8
M_DATA_A9	AR3	SA_DQ_9
M_DATA_A10	AR4	SA_DQ_10
M_DATA_A11	AN2	SA_DQ_11
M_DATA_A12	AR2	SA_DQ_12
M_DATA_A13	AR1	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AW3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AU2	SA_DQ_19
M_DATA_A20	AU3	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AV5	SA_DQ_23
M_DATA_A24	AV7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AW7	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AW35	SA_DQ_35
M_DATA_A36	AW35	SA_DQ_36
M_DATA_A37	AY36	SA_DQ_37
M_DATA_A38	AU38	SA_DQ_38
M_DATA_A39	AU37	SA_DQ_39
M_DATA_A40	AR37	SA_DQ_40
M_DATA_A41	AN36	SA_DQ_41
M_DATA_A42	AN37	SA_DQ_42
M_DATA_A43	AR39	SA_DQ_43
M_DATA_A44	AR38	SA_DQ_44
M_DATA_A45	AN38	SA_DQ_45
M_DATA_A46	AN40	SA_DQ_46
M_DATA_A47	AL40	SA_DQ_47
M_DATA_A48	AL37	SA_DQ_48
M_DATA_A49	AJ38	SA_DQ_49
M_DATA_A50	AJ37	SA_DQ_50
M_DATA_A51	AJ38	SA_DQ_51
M_DATA_A52	AJ38	SA_DQ_52
M_DATA_A53	AJ39	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AG40	SA_DQ_55
M_DATA_A56	AG37	SA_DQ_56
M_DATA_A57	AE38	SA_DQ_57
M_DATA_A58	AE37	SA_DQ_58
M_DATA_A59	AG39	SA_DQ_59
M_DATA_A60	AG38	SA_DQ_60
M_DATA_A61	AE39	SA_DQ_61
M_DATA_A62	AE38	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV38	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

DDR_0
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SKT_H2_CRB

DDR3 CH.A

BALLMAP_REV=1.4

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

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SA_ECC_CB_1
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SA_ECC_CB_3
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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

SM_DRAMRST#

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SA_DQS#_8

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DDR3 CH.A

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

SM_DRAMRST#

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DDR_0
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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

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DDR3 CH.A

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DDR3 CH.A

SM_DRAMRST#

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DDR3 CH.A

SM_DRAMRST#

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SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

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DDR3 CH.A

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

MAX 112A		MAX 112A	
In	CPU_VCORE	In	CPU_VCORE
A12	VCC_001	F32	VCC_082
A13	VCC_002	F33	VCC_083
A14	VCC_003	F34	VCC_084
A15	VCC_004	G18	VCC_085
A16	VCC_005	G19	VCC_086
A18	VCC_006	G21	VCC_087
A24	VCC_007	G22	VCC_088
A25	VCC_008	G23	VCC_089
A27	VCC_009	G24	VCC_090
A28	VCC_010	G25	VCC_091
B15	VCC_011	G27	VCC_092
B16	VCC_012	G28	VCC_093
B18	VCC_013	G30	VCC_094
B24	VCC_014	G31	VCC_095
B25	VCC_015	G32	VCC_096
B27	VCC_016	G33	VCC_097
B28	VCC_017	H13	VCC_098
B30	VCC_018	H14	VCC_099
B31	VCC_019	H15	VCC_100
B33	VCC_020	H16	VCC_101
B34	VCC_021	H18	VCC_102
C15	VCC_022	H19	VCC_103
C16	VCC_023	H21	VCC_104
C18	VCC_024	H22	VCC_105
C19	VCC_025	H24	VCC_106
C21	VCC_026	H25	VCC_107
C22	VCC_027	H27	VCC_108
C24	VCC_028	H28	VCC_109
C25	VCC_029	H30	VCC_110
C27	VCC_030	H31	VCC_111
C28	VCC_031	H32	VCC_112
C30	VCC_032	I12	VCC_113
C31	VCC_033	I15	VCC_114
C33	VCC_034	I16	VCC_115
C34	VCC_035	I18	VCC_116
C36	VCC_036	I19	VCC_117
D13	VCC_037	I21	VCC_118
D14	VCC_038	I22	VCC_119
D15	VCC_039	I24	VCC_120
D16	VCC_040	I25	VCC_121
D18	VCC_041	I27	VCC_122
D19	VCC_042	I28	VCC_123
D21	VCC_043	I30	VCC_124
D22	VCC_044	K15	VCC_125
D24	VCC_045	K16	VCC_126
D25	VCC_046	K18	VCC_127
D27	VCC_047	K19	VCC_128
D28	VCC_048	K21	VCC_129
D30	VCC_049	K22	VCC_130
D31	VCC_050	K24	VCC_131
D33	VCC_051	K25	VCC_132
D34	VCC_052	K27	VCC_133
D35	VCC_053	K28	VCC_134
D36	VCC_054	K30	VCC_135
E15	VCC_055	L12	VCC_136
E16	VCC_056	L13	VCC_137
E18	VCC_057	L14	VCC_138
E19	VCC_058	L15	VCC_139
E21	VCC_059	L16	VCC_140
E22	VCC_060	L18	VCC_141
E24	VCC_061	L19	VCC_142
E25	VCC_062	L21	VCC_143
E27	VCC_063	L22	VCC_144
E28	VCC_064	L24	VCC_145
E30	VCC_065	L25	VCC_146
E31	VCC_066	L27	VCC_147
E33	VCC_067	L28	VCC_148
E34	VCC_068	L30	VCC_149
E35	VCC_069	M14	VCC_150
F15	VCC_070	M15	VCC_151
F16	VCC_071	M16	VCC_152
F18	VCC_072	M18	VCC_153
F19	VCC_073	M19	VCC_154
F21	VCC_074	M21	VCC_155
F22	VCC_075	M22	VCC_156
F24	VCC_076	M24	VCC_157
F25	VCC_077	M25	VCC_158
F27	VCC_078	M27	VCC_159
F28	VCC_079	M28	VCC_160
F30	VCC_080	M30	VCC_161
F31	VCC_081		

BALLMAP_REV=1.4

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SKT_H2_CRB

1.05V/1.00V
MAX 8.8A

MAX 112A		MAX 112A	
In	CPU_VCORE	In	CPU_VCORE
A12	VCC_001	F32	VCC_082
A13	VCC_002	F33	VCC_083
A14	VCC_003	F34	VCC_084
A15	VCC_004	G18	VCC_085
A16	VCC_005	G19	VCC_086
A18	VCC_006	G21	VCC_087
A24	VCC_007	G22	VCC_088
A25	VCC_008	G23	VCC_089
A27	VCC_009	G24	VCC_090
A28	VCC_010	G25	VCC_091
B15	VCC_011	G27	VCC_092
B16	VCC_012	G28	VCC_093
B18	VCC_013	G30	VCC_094
B24	VCC_014	G31	VCC_095
B25	VCC_015	G32	VCC_096
B27	VCC_016	G33	VCC_097
B28	VCC_017	H13	VCC_098
B30	VCC_018	H14	VCC_099
B31	VCC_019	H15	VCC_100
B33	VCC_020	H16	VCC_101
B34	VCC_021	H18	VCC_102
C15	VCC_022	H19	VCC_103
C16	VCC_023	H21	VCC_104
C18	VCC_024	H22	VCC_105
C19	VCC_025	H24	VCC_106
C21	VCC_026	H25	VCC_107
C22	VCC_027	H27	VCC_108
C24	VCC_028	H28	VCC_109
C25	VCC_029	H30	VCC_110
C27	VCC_030	H31	VCC_111
C28	VCC_031	H32	VCC_112
C30	VCC_032	I12	VCC_113
C31	VCC_033	I15	VCC_114
C33	VCC_034	I16	VCC_115
C34	VCC_035	I18	VCC_116
C36	VCC_036	I19	VCC_117
D13	VCC_037	I21	VCC_118
D14	VCC_038	I22	VCC_119
D15	VCC_039	I24	VCC_120
D16	VCC_040	I25	VCC_121
D18	VCC_041	I27	VCC_122
D19	VCC_042	I28	VCC_123
D21	VCC_043	I30	VCC_124
D22	VCC_044	K15	VCC_125
D24	VCC_045	K16	VCC_126
D25	VCC_046	K18	VCC_127
D27	VCC_047	K19	VCC_128
D28	VCC_048	K21	VCC_129
D30	VCC_049	K22	VCC_130
D31	VCC_050	K24	VCC_131
D33	VCC_051	K25	VCC_132
D34	VCC_052	K27	VCC_133
D35	VCC_053	K28	VCC_134
D36	VCC_054	K30	VCC_135
E15	VCC_055	L12	VCC_136
E16	VCC_056	L13	VCC_137
E18	VCC_057	L14	VCC_138
E19	VCC_058	L15	VCC_139
E21	VCC_059	L16	VCC_140
E22	VCC_060	L18	VCC_141
E24	VCC_061	L19	VCC_142
E25	VCC_062	L21	VCC_143
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E28	VCC_064	L24	VCC_145
E30	VCC_065	L25	VCC_146
E31	VCC_066	L27	VCC_147
E33	VCC_067	L28	VCC_148
E34	VCC_068	L30	VCC_149
E35	VCC_069	M14	VCC_150
F15	VCC_070	M15	VCC_151
F16	VCC_071	M16	VCC_152
F18	VCC_072	M18	VCC_153
F19	VCC_073	M19	VCC_154
F21	VCC_074	M21	VCC_155
F22	VCC_075	M22	VCC_156
F24	VCC_076	M24	VCC_157
F25	VCC_077	M25	VCC_158
F27	VCC_078	M27	VCC_159
F28	VCC_079	M28	VCC_160
F30	VCC_080	M30	VCC_161
F31	VCC_081		

BALLMAP_REV=1.4

POWER
7 OF 10

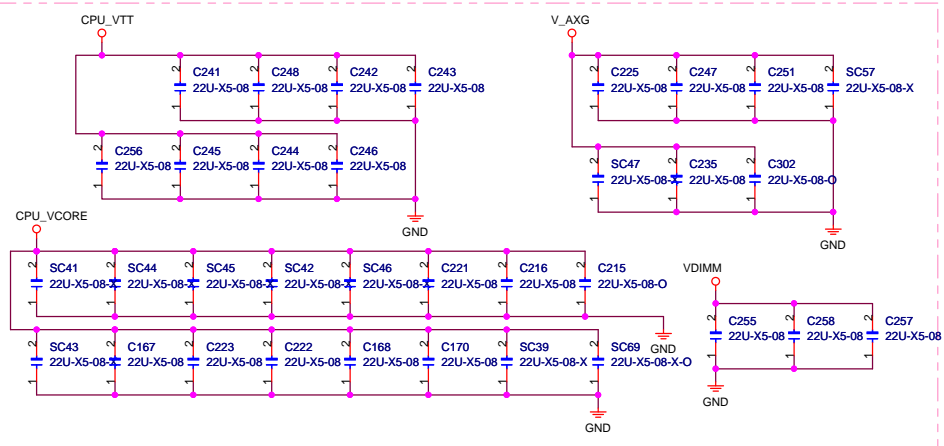
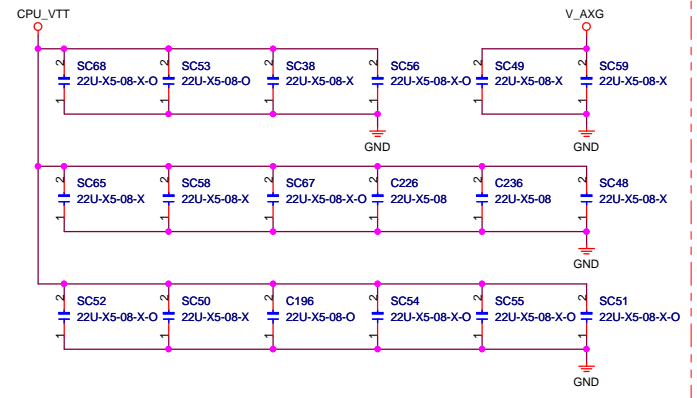
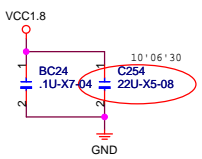
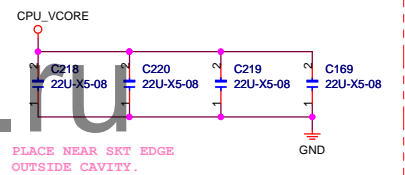
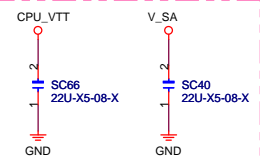
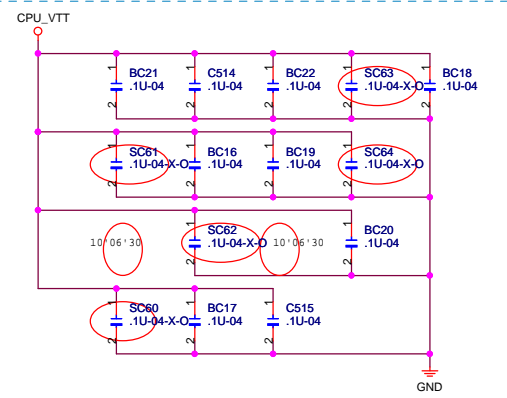
1.5V
MAX 4.5A

MAX 35A		MAX 35A	
In	V_AXG	In	V_AXG
A13	VCCIO_01	AJ13	VCCIO_01
A14	VCCIO_02	AJ14	VCCIO_02
A15	VCCIO_03	AJ15	VCCIO_03
A16	VCCIO_04	AJ16	VCCIO_04
A18	VCCIO_05	AJ18	VCCIO_05
A24	VCCIO_06	AJ24	VCCIO_06
A25	VCCIO_07	AJ25	VCCIO_07
A27	VCCIO_08	AJ27	VCCIO_08
A28	VCCIO_09	AJ28	VCCIO_09
B15	VCCIO_10	AJ30	VCCIO_10
B16	VCCIO_11	AJ31	VCCIO_11
B18	VCCIO_12	AJ32	VCCIO_12
B24	VCCIO_13	AJ33	VCCIO_13
B25	VCCIO_14	AJ34	VCCIO_14
B27	VCCIO_15	AJ35	VCCIO_15
B28	VCCIO_16	AJ36	VCCIO_16
B30	VCCIO_17	AJ37	VCCIO_17
B31	VCCIO_18	AJ38	VCCIO_18
B33	VCCIO_19	AJ39	VCCIO_19
B34	VCCIO_20	AJ40	VCCIO_20
C15	VCCIO_21	AJ41	VCCIO_21
C16	VCCIO_22	AJ42	VCCIO_22
C18	VCCIO_23	AJ43	VCCIO_23
C19	VCCIO_24	AJ44	VCCIO_24
C21	VCCIO_25	AJ45	VCCIO_25
C22	VCCIO_26	AJ46	VCCIO_26
C24	VCCIO_27	AJ47	VCCIO_27
C25	VCCIO_28	AJ48	VCCIO_28
C27	VCCIO_29	AJ49	VCCIO_29
C28	VCCIO_30	AJ50	VCCIO_30
C30	VCCIO_31		
C31	VCCIO_32		
C33	VCCIO_33		
C34	VCCIO_34		
C36	VCCIO_35		
D13	VCCIO_36		
D14	VCCIO_37		
D15	VCCIO_38		
D16	VCCIO_39		
D18	VCCIO_40		
D19	VCCIO_41		
D21	VCCIO_42		
D22	VCCIO_43		
D24	VCCIO_44		
D25	VCCIO_45		
D27	VCCIO_46		
D28	VCCIO_47		
D30	VCCIO_48		
D31	VCCIO_49		
D33	VCCIO_50		
D34	VCCIO_51		
D35	VCCIO_52		
D36	VCCIO_53		
E15	VCCIO_54		
E16	VCCIO_55		
E18	VCCIO_56		
E19	VCCIO_57		
E21	VCCIO_58		
E22	VCCIO_59		
E24	VCCIO_60		
E25	VCCIO_61		
E27	VCCIO_62		
E28	VCCIO_63		
E30	VCCIO_64		
E31	VCCIO_65		
E33	VCCIO_66		
E34	VCCIO_67		
E35	VCCIO_68		
F15	VCCIO_69		
F16	VCCIO_70		
F18	VCCIO_71		
F19	VCCIO_72		
F21	VCCIO_73		
F22	VCCIO_74		
F24	VCCIO_75		
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F30	VCCIO_79		
F31	VCCIO_80		

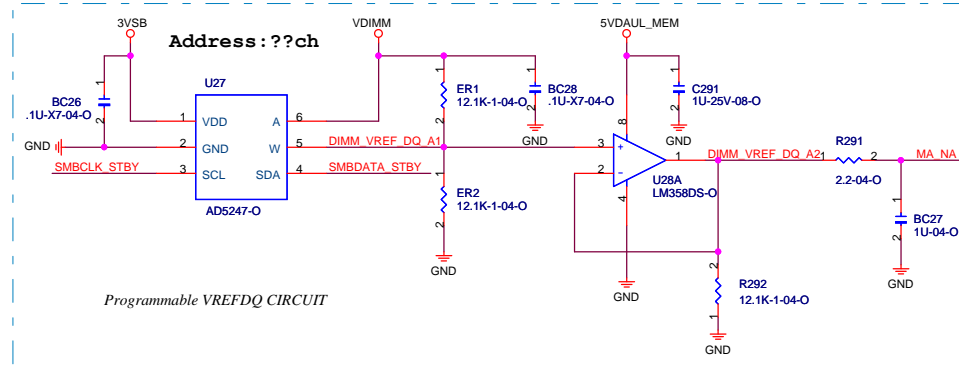
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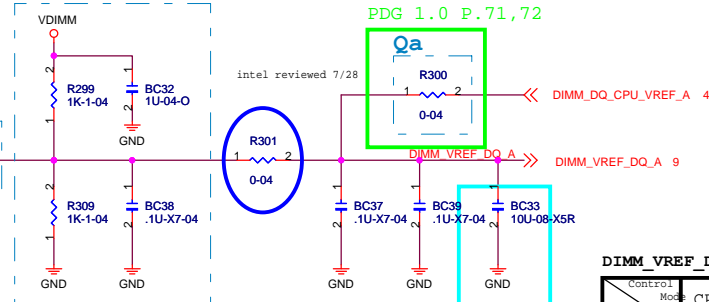
SKT_H2_CRB



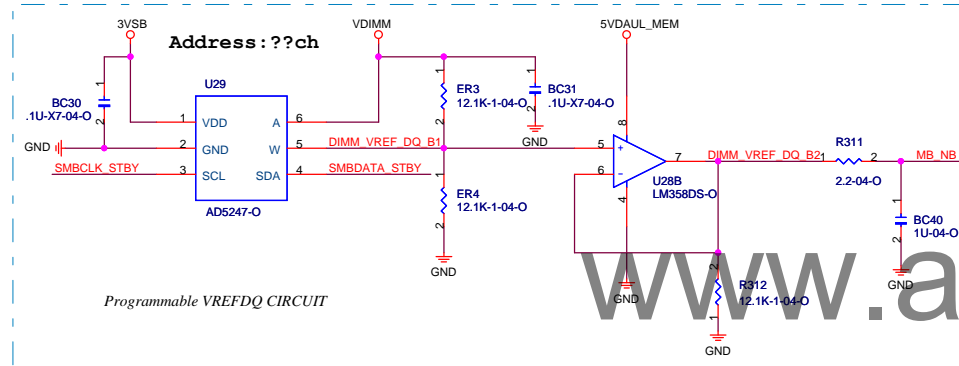
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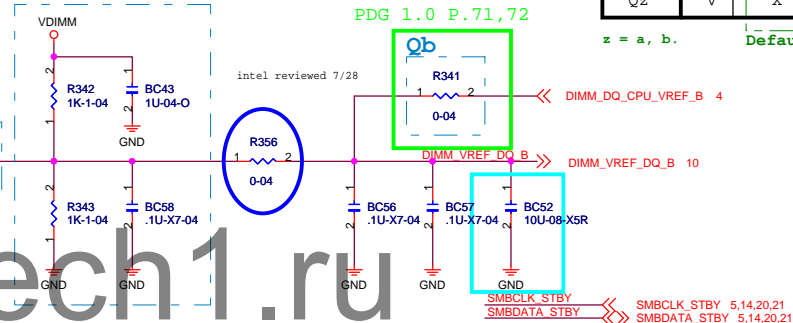
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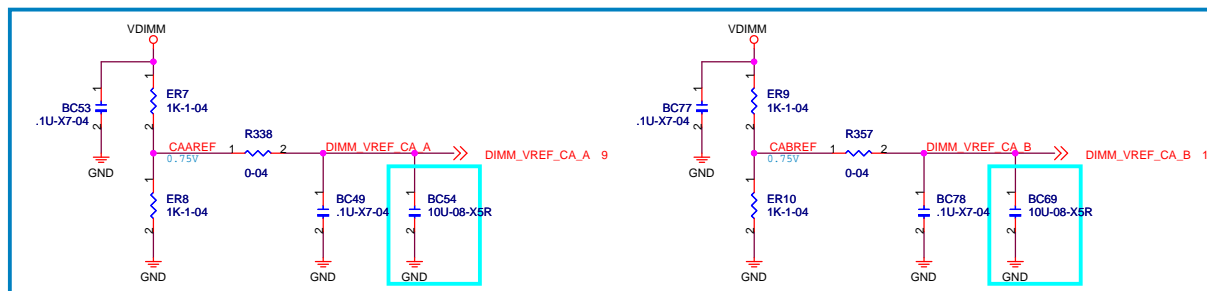
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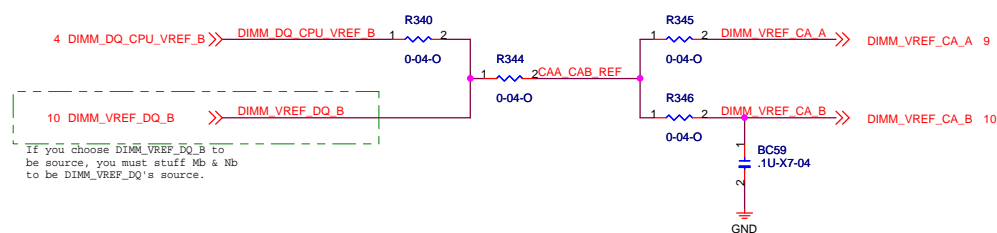
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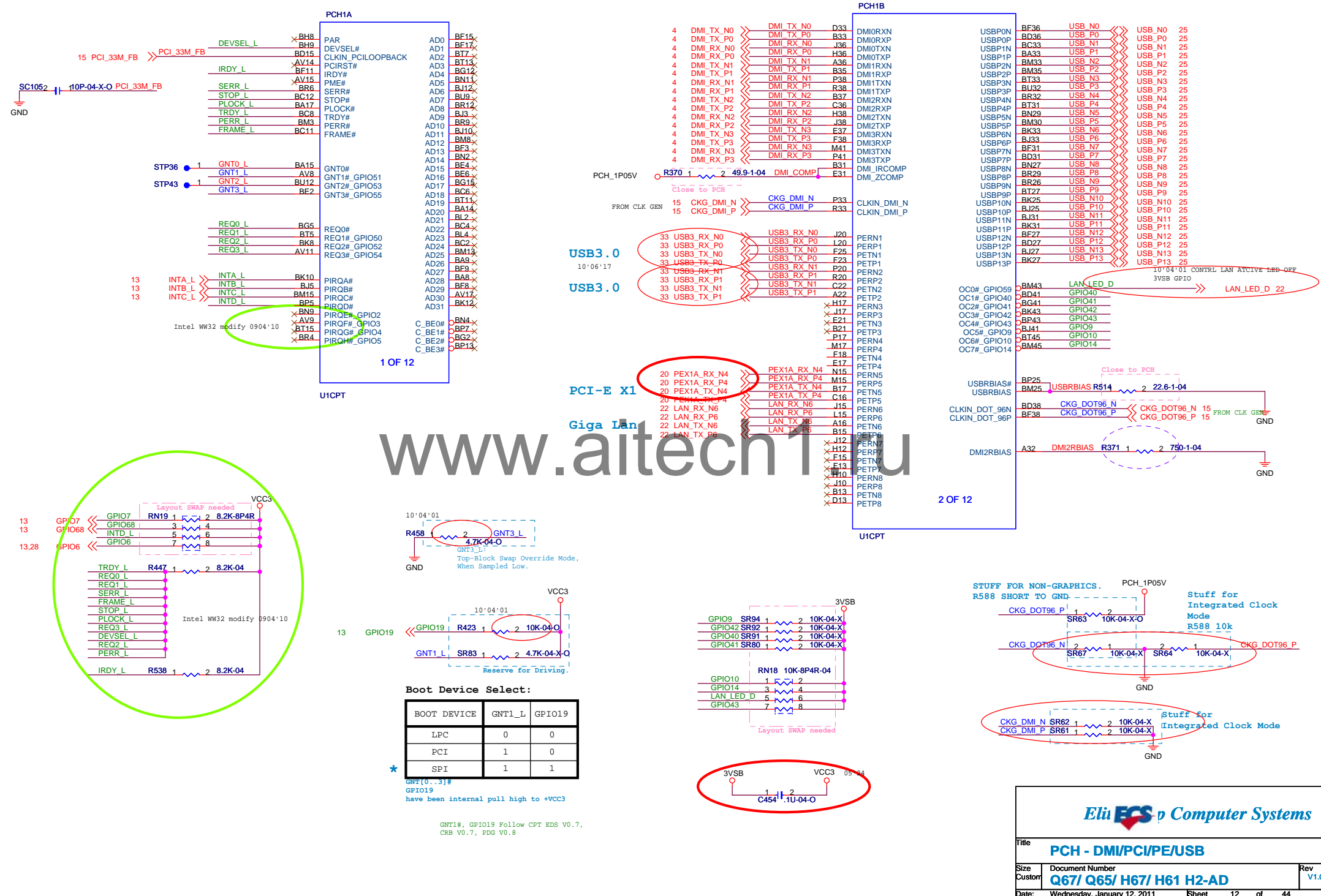
DIMM_VREF_DQ Control Circuit



DIMM_VREF_CA Circuit



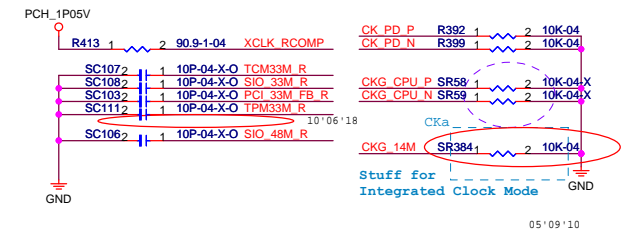
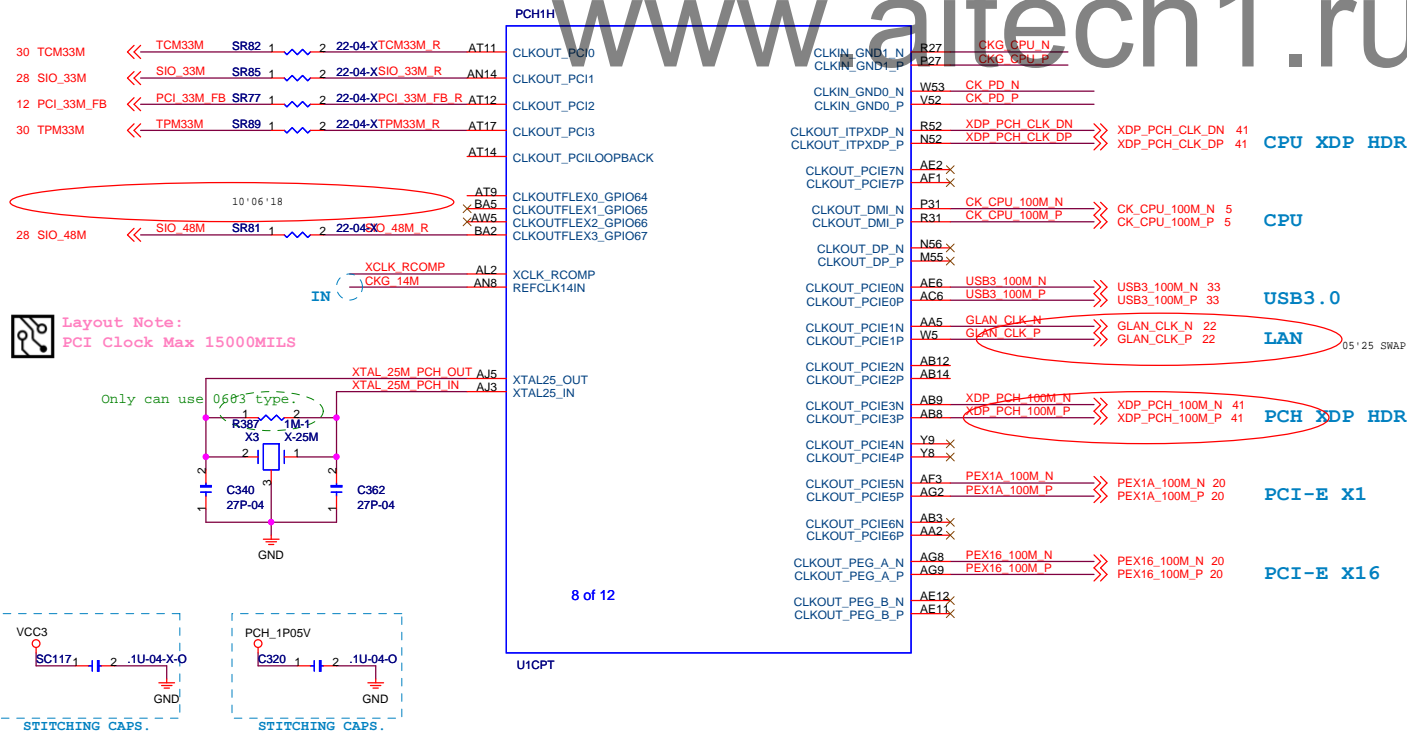
www.aitech1u



0908'10 TAKE OFF CLK GEN

CLK GEN.Seligo SLG421 Circuit.

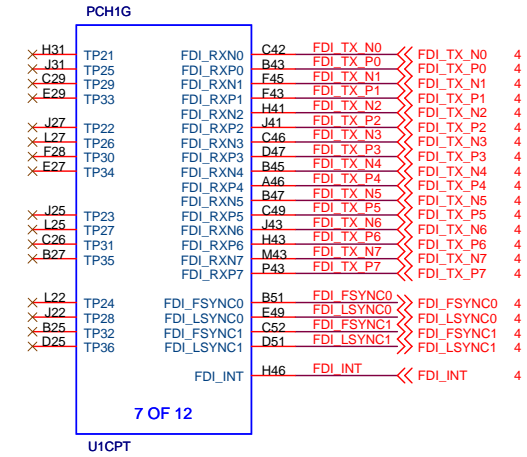
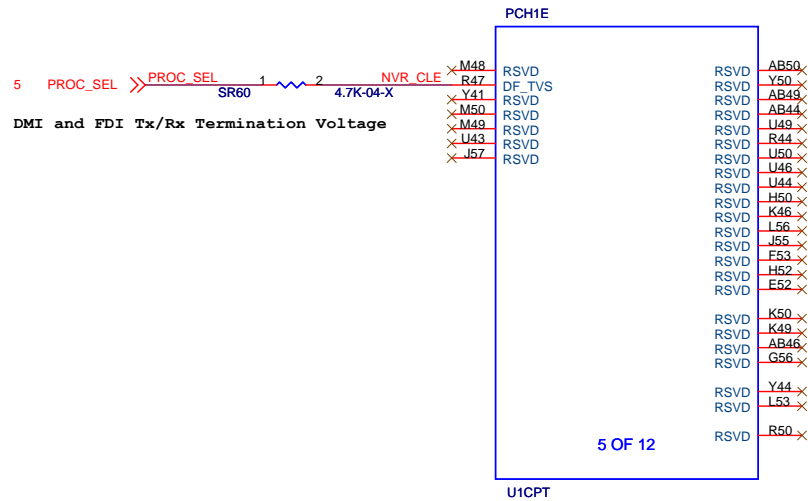
www.aitech1.ru



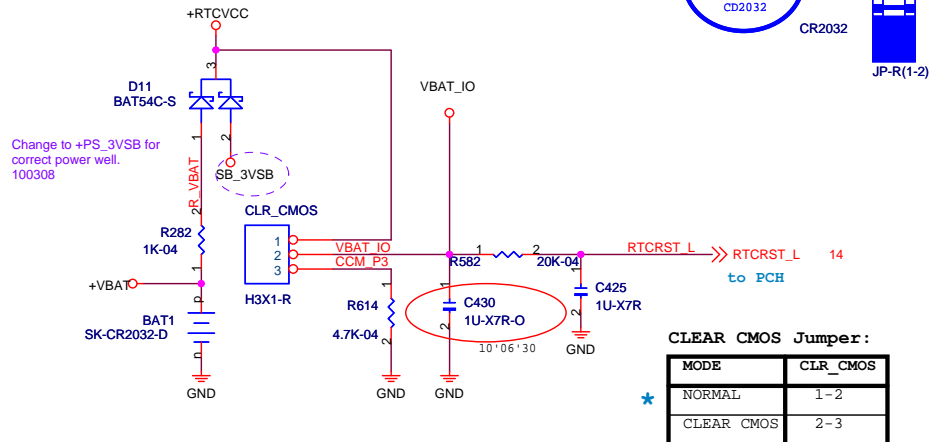
Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	x	v
Buffer Through Mode	y	x

Elitegroup Computer Systems

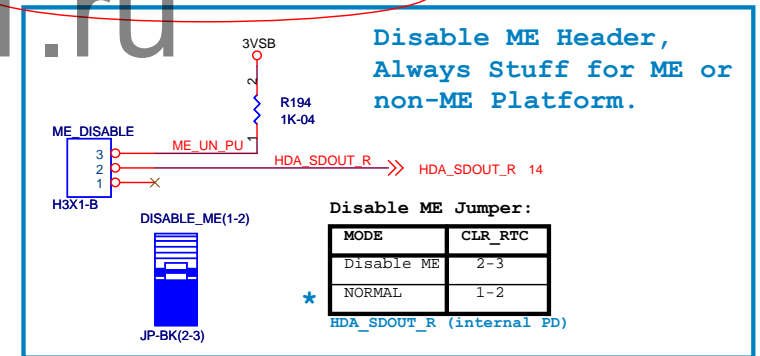
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Size	Document Number	Rev	
Custom	Q67/ Q65/ H67/ H61 H2-AD	V1.0	
Date:	Wednesday, January 12, 2011	Sheet	15 of 44



CLR_CMOS



04'20'10 CHANGE JUMPER DEFINE

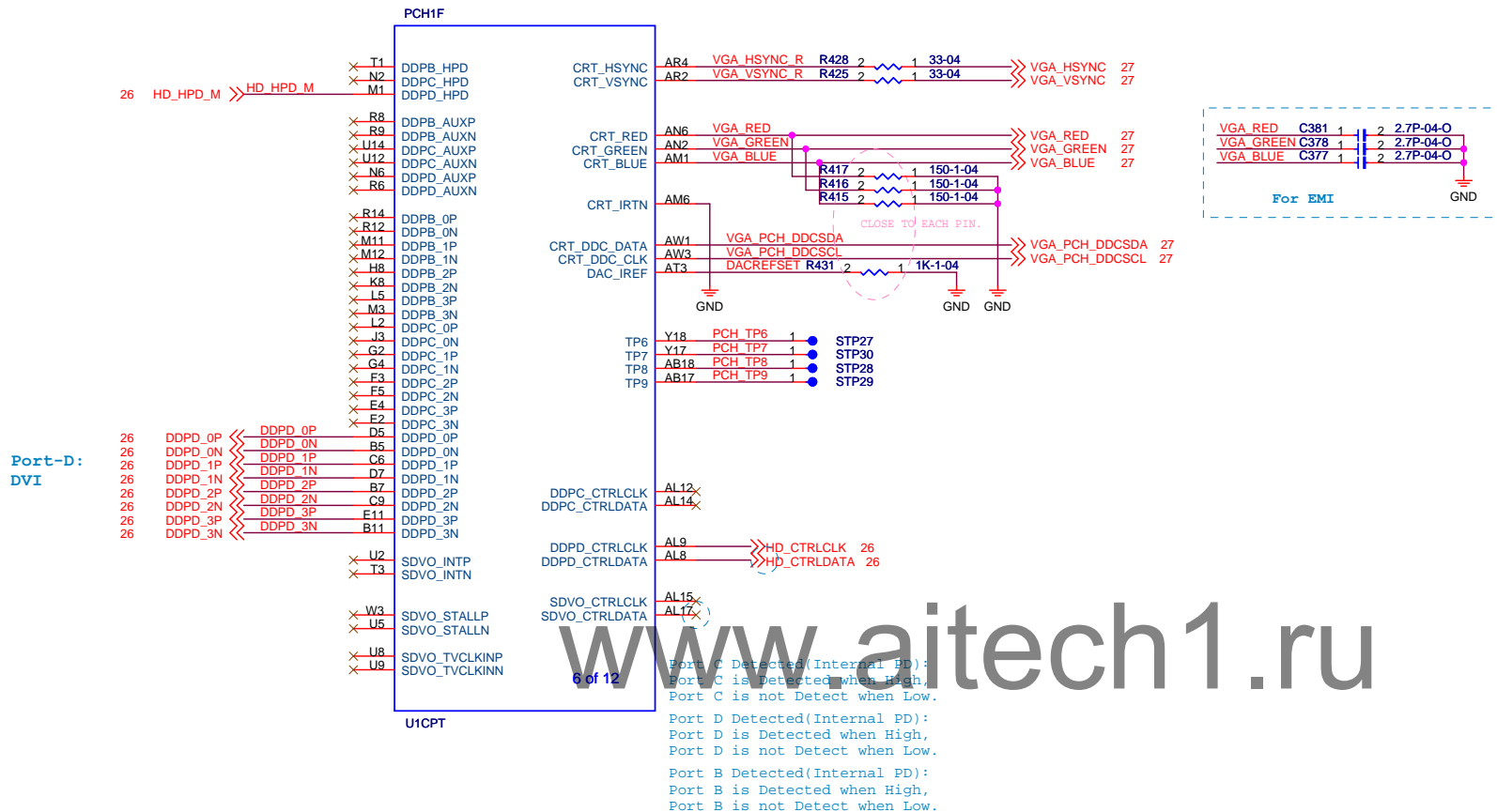


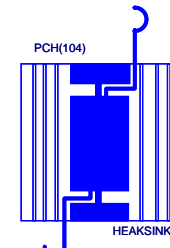
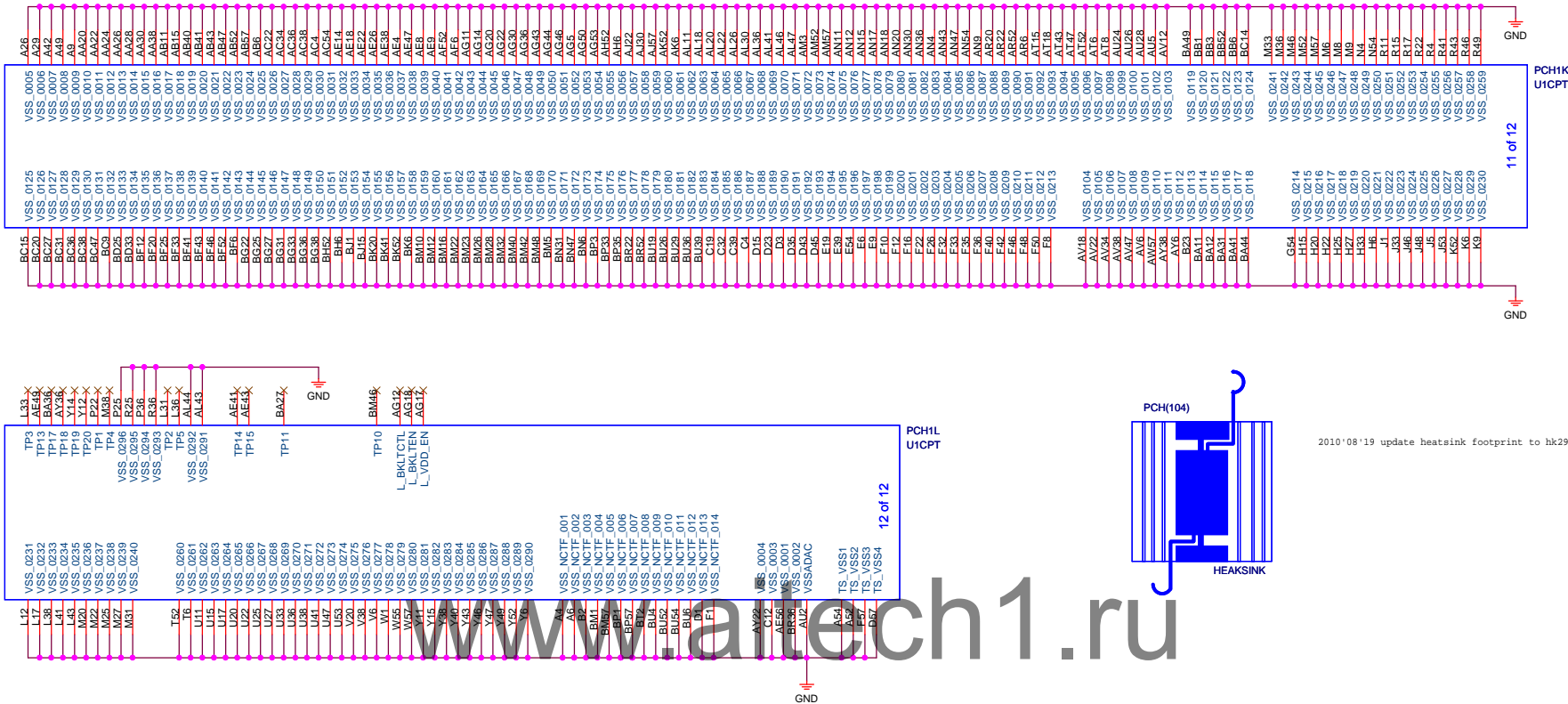
Elitegroup Computer Systems

Title **PCH - NVRAM/FDI, CLR_CMOS**

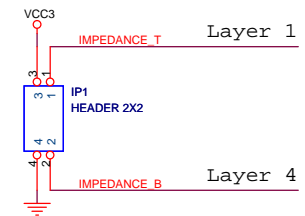
Size B Document Number **Q67/ Q65/ H67/ H61 H2-AD** Rev V1.0

Date: Wednesday, January 12, 2011 Sheet 16 of 44

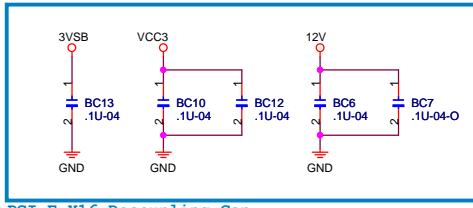
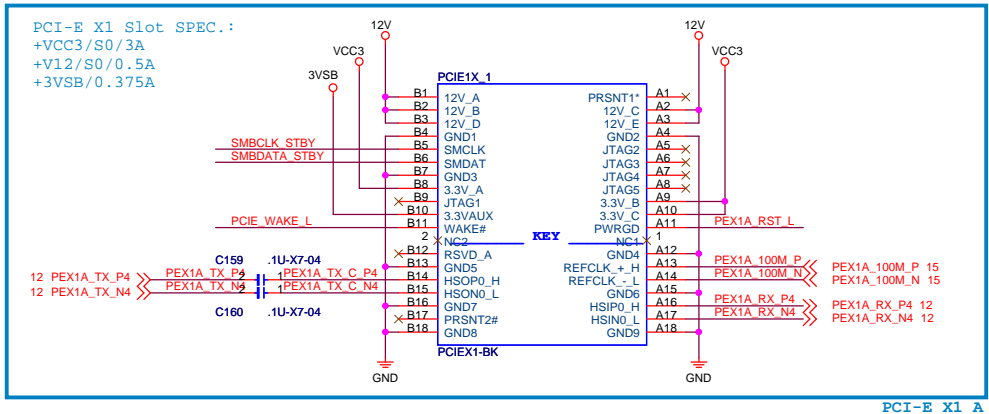
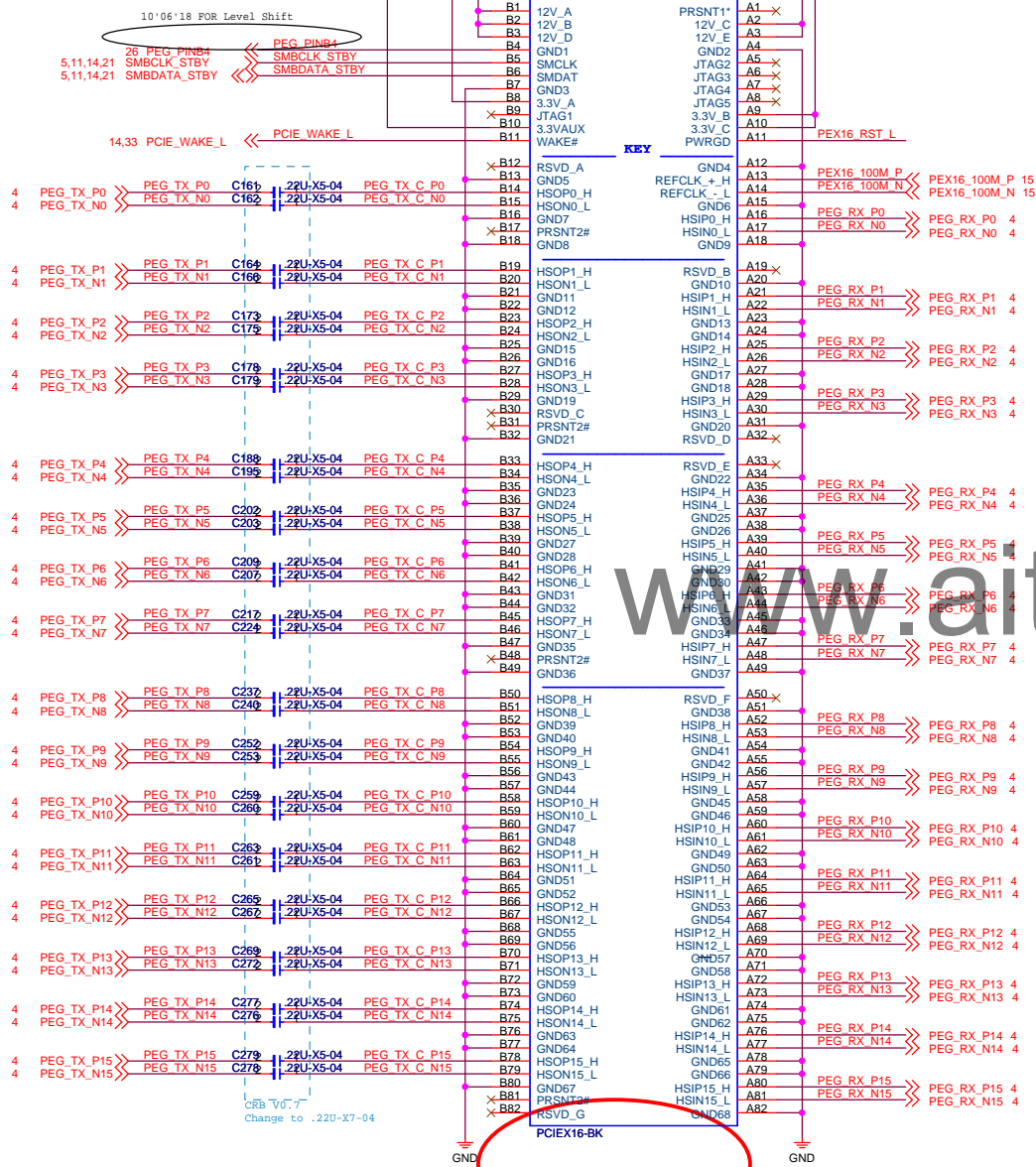




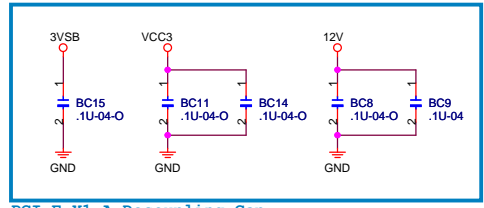
2010'08'19 update heatsink footprint to hk29d4x30d7_pt40d11x21



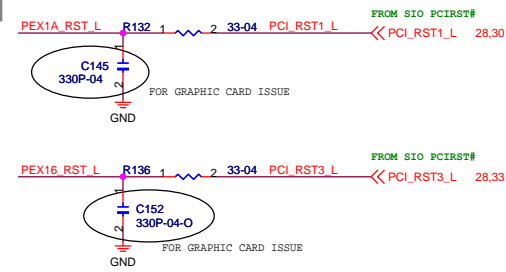
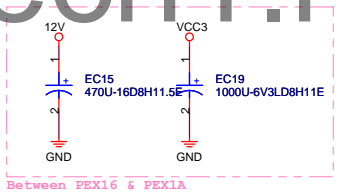
PCI-E X16 Slot SPEC.:
 +VCC3/S0/3A
 +V12/S0/5.5A
 +3VSB/0.375A



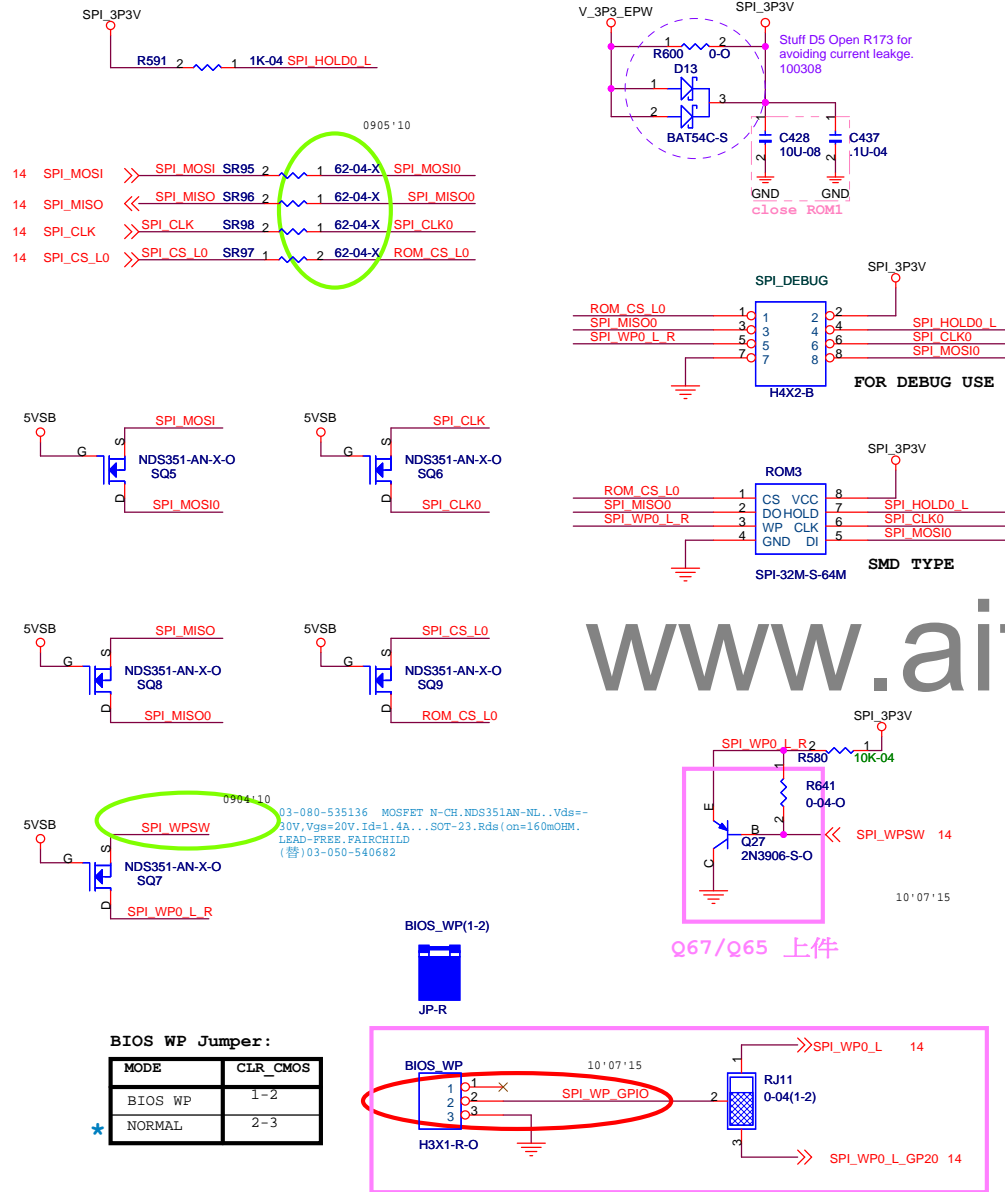
PCI-E X16 Decoupling Cap.



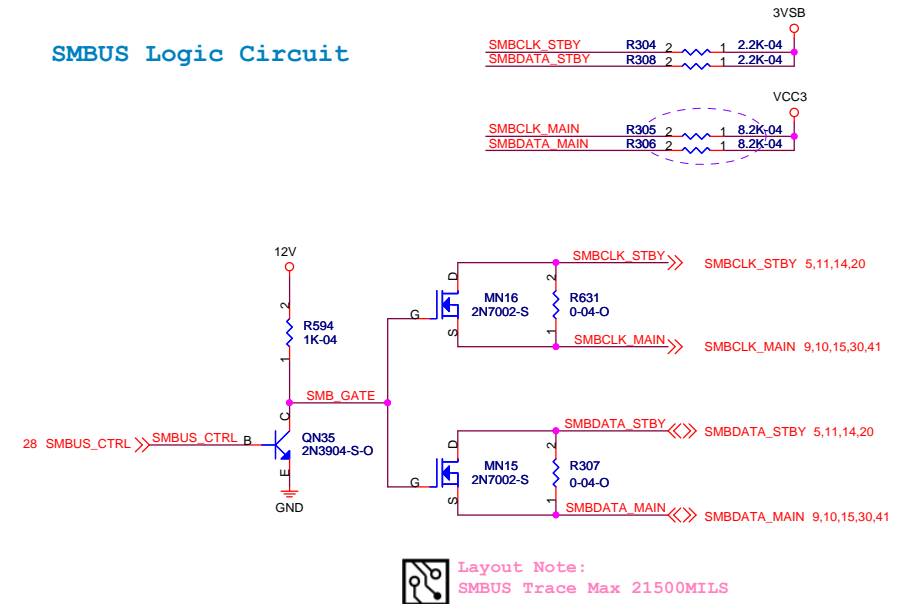
PCI-E X1 A Decoupling Cap.



SPI ROM Circuit

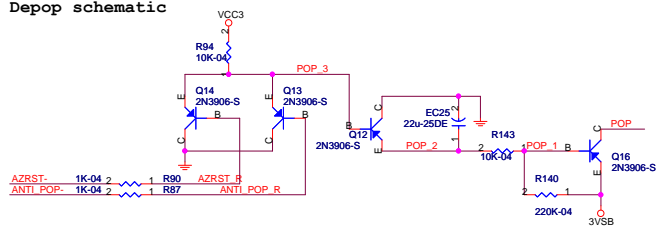


SMBUS Logic Circuit

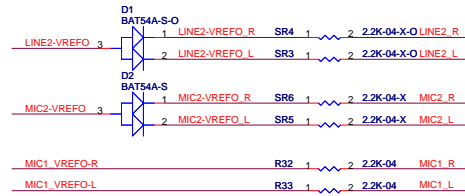


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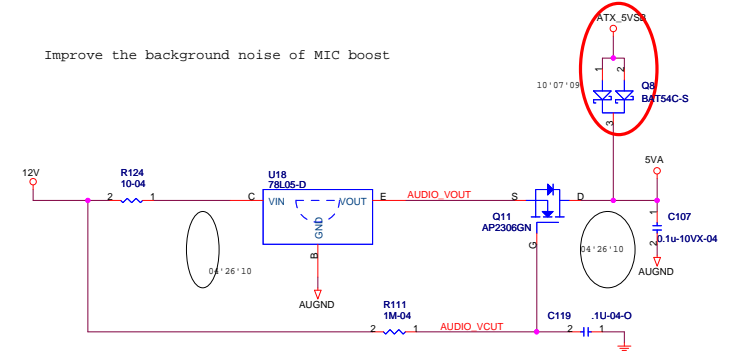
Depop schematic



MIC Bias



Improve the background noise of MIC boost



Resistors Networks

Place near Chip

R49 1 2 39.2K-1-04

R50 1 2 20K-1-04

SAR1 75-04-X

SAR2 75-04-X

SAC1 22U-X5-12-XFRONT_L

SAC2 22U-X5-12-XFRONT_R

1109'10

10'06'23 change to MLCC

ACODEC1

AVDD1

AVDD2

AVSS2

AVSS1

AVSS0

AVSS3

AVSS4

AVSS5

AVSS6

AVSS7

AVSS8

AVSS9

AVSS10

AVSS11

AVSS12

AVSS13

AVSS14

AVSS15

AVSS16

AVSS17

AVSS18

AVSS19

AVSS20

AVSS21

AVSS22

AVSS23

AVSS24

AVSS25

AVSS26

AVSS27

AVSS28

AVSS29

AVSS30

AVSS31

AVSS32

AVSS33

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AVSS198

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AVSS200

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AVSS202

AVSS203

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AVSS205

AVSS206

AVSS207

AVSS208

AVSS209

AVSS210

AVSS211

AVSS212

AVSS213

AVSS214

AVSS215

AVSS216

AVSS217

AVSS218

AVSS219

AVSS220

AVSS221

AVSS222

AVSS223

AVSS224

AVSS225

AVSS226

AVSS227

AVSS228

AVSS229

AVSS230

AVSS231

AVSS232

AVSS233

AVSS234

AVSS235

AVSS236

AVSS237

AVSS238

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AVSS248

AVSS249

AVSS250

AVSS251

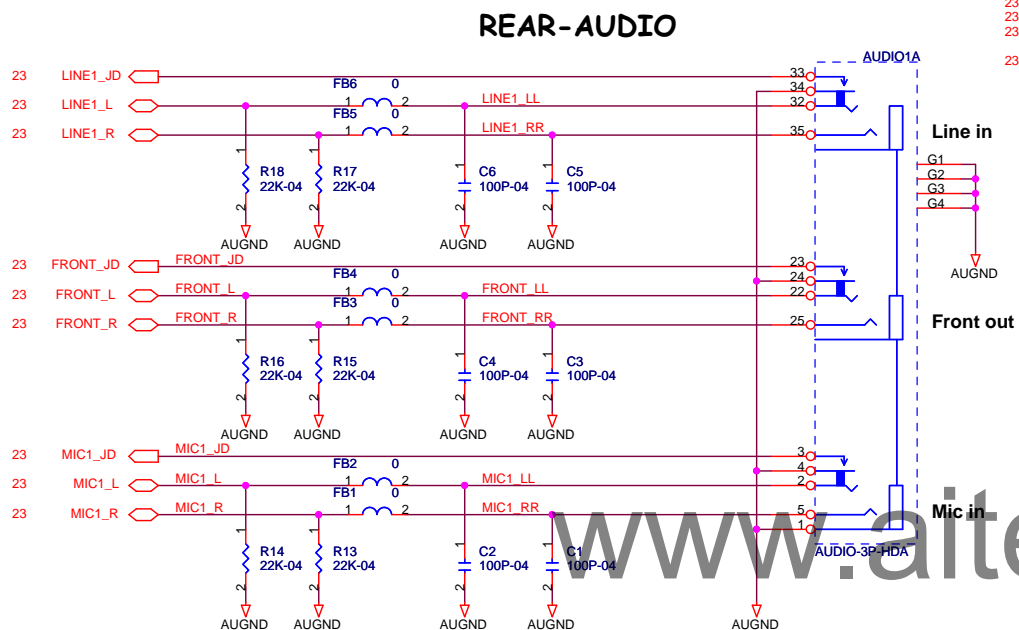
AVSS252

AVSS253

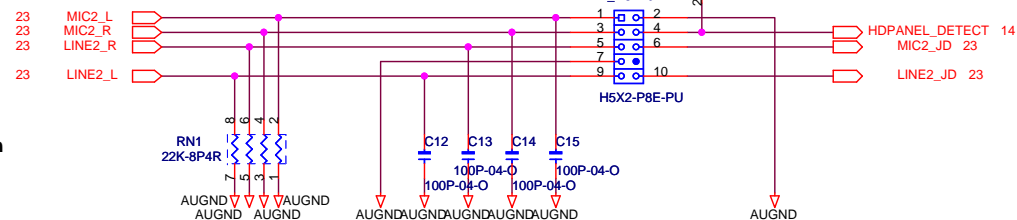
AVSS254

AVSS255

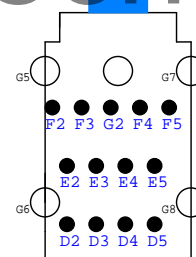
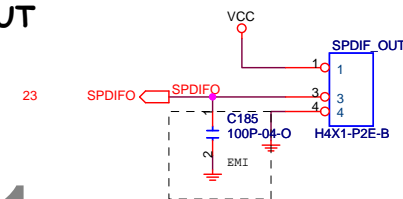
AVSS256</



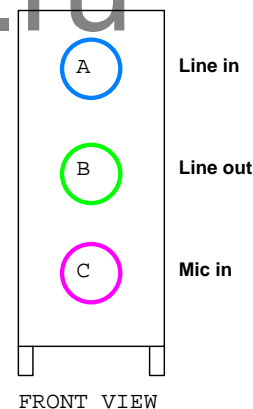
FRONT-AUDIO



SPDIF-OUT



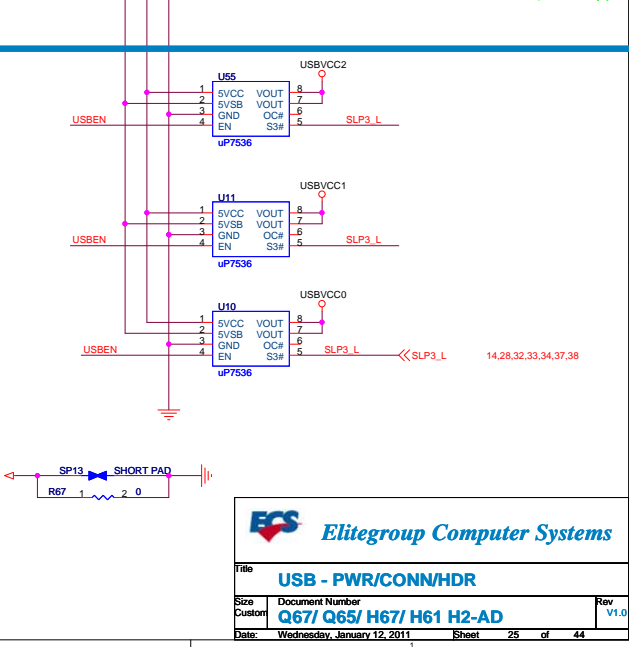
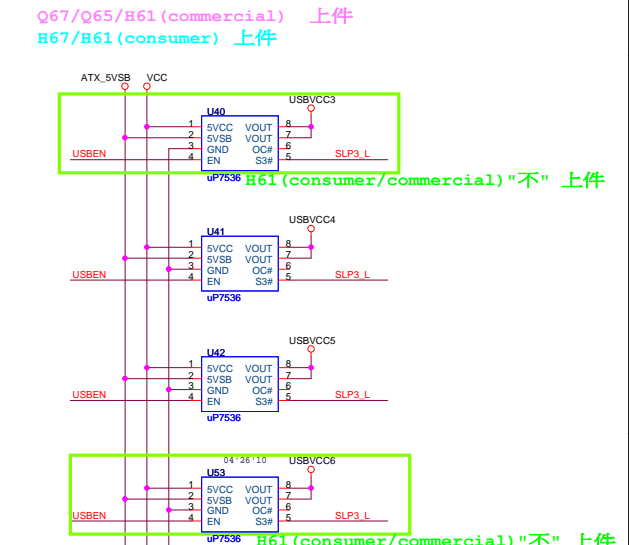
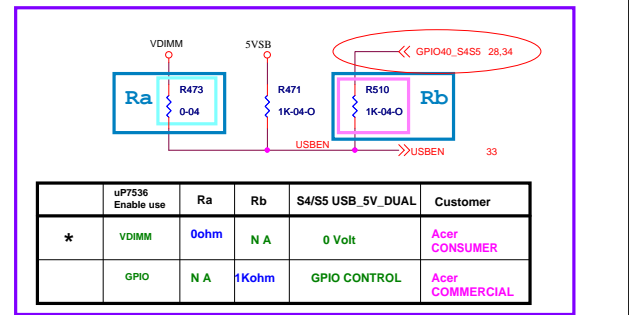
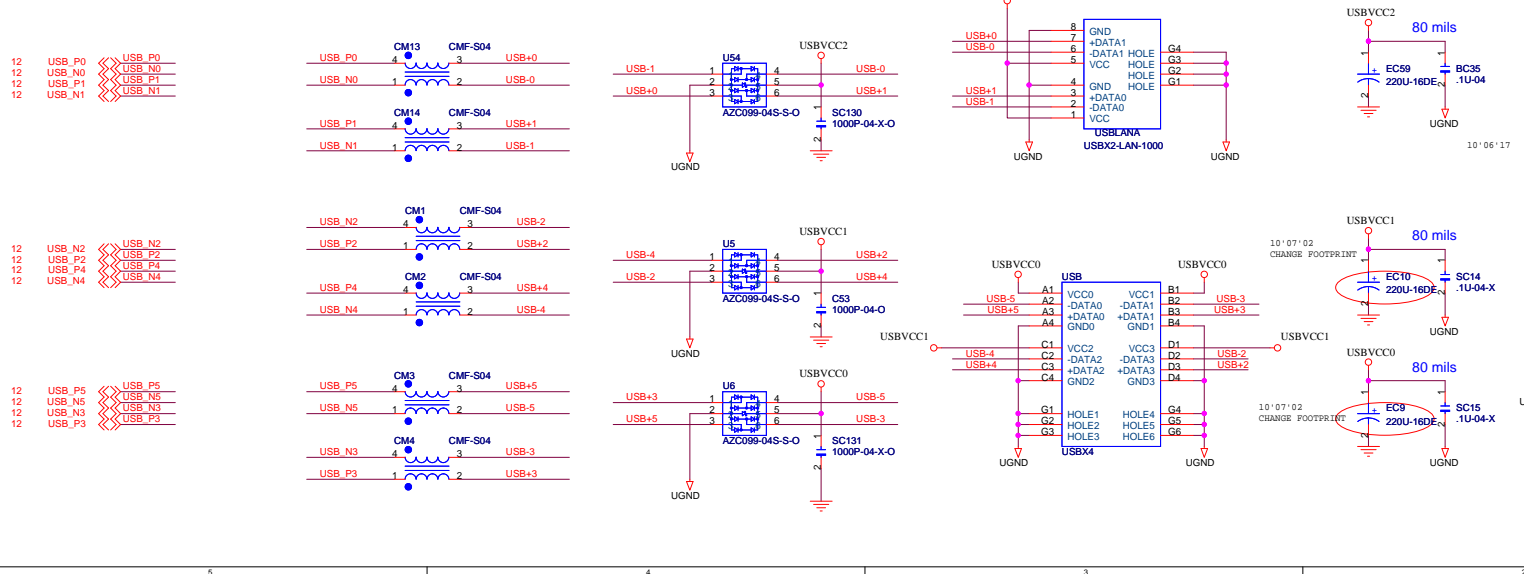
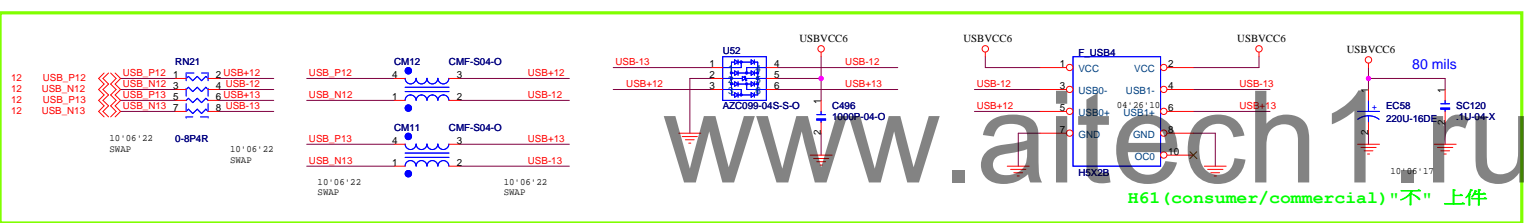
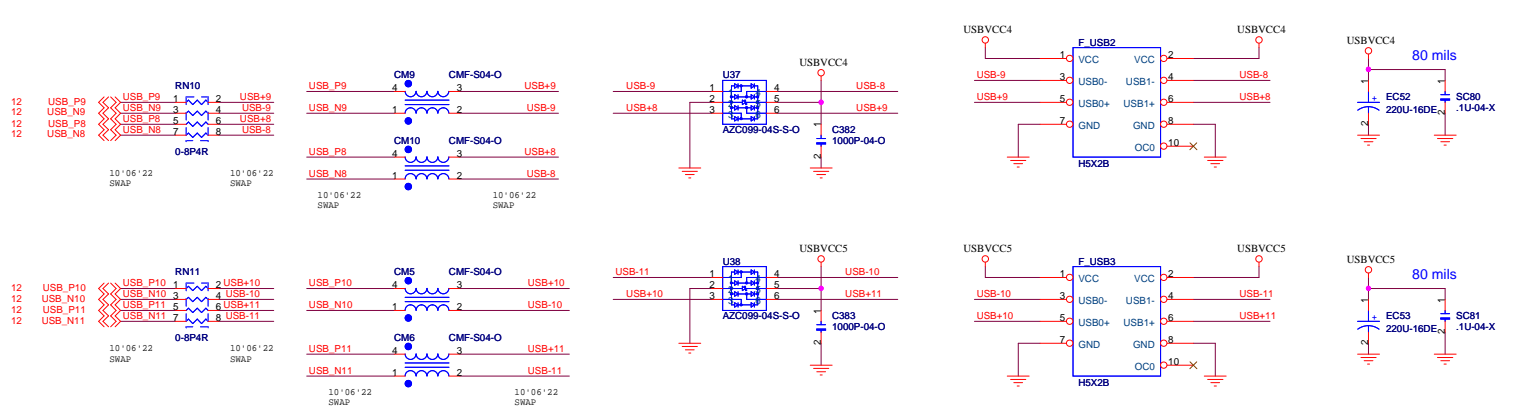
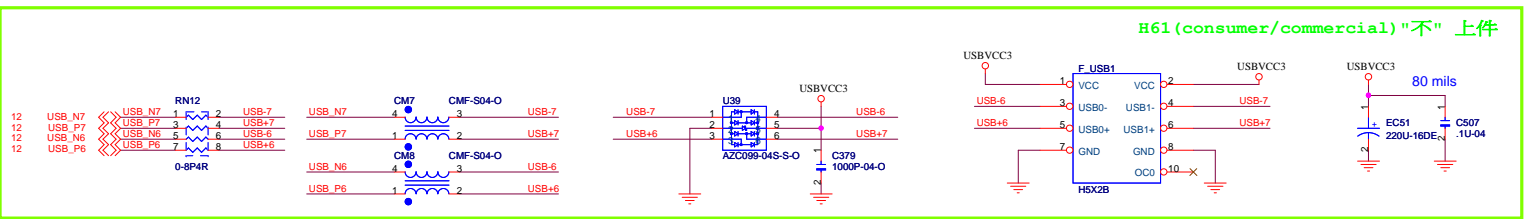
TOP VIEW



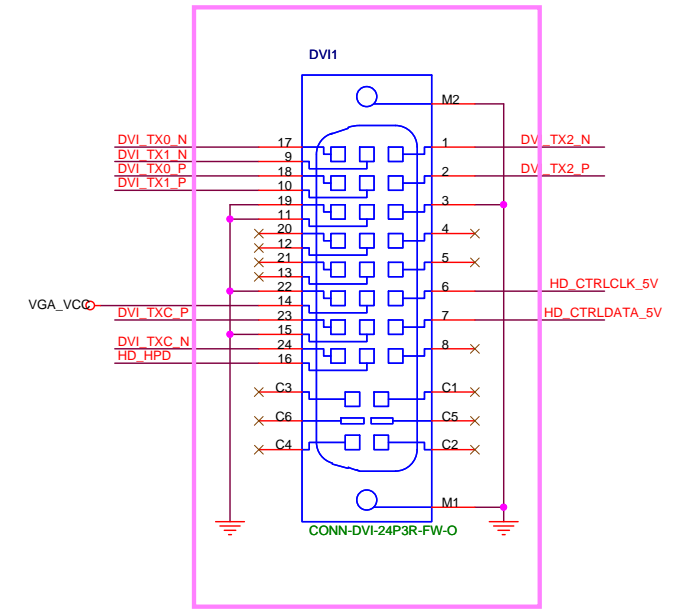
FRONT VIEW

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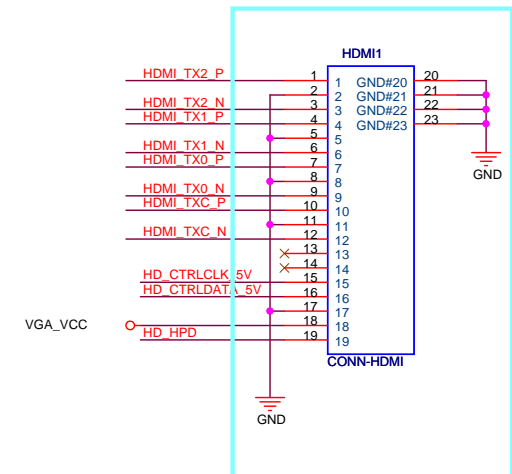
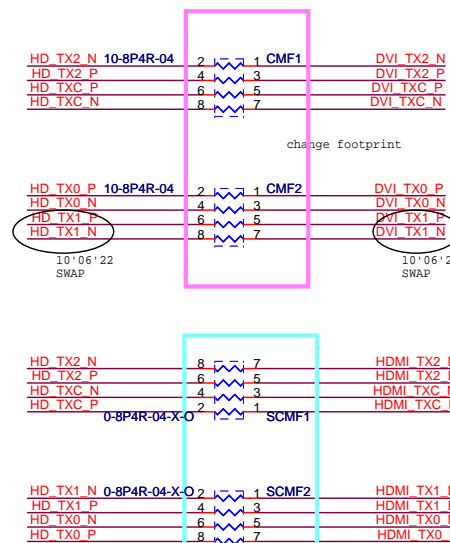
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AUDIO ALC662 (PANEL)		
Size	Document Number	Rev
B	Q67/ Q65/ H67/ H61 H2-AD	V1.0
Date:	Wednesday, January 12, 2011	Sheet 24 of 44



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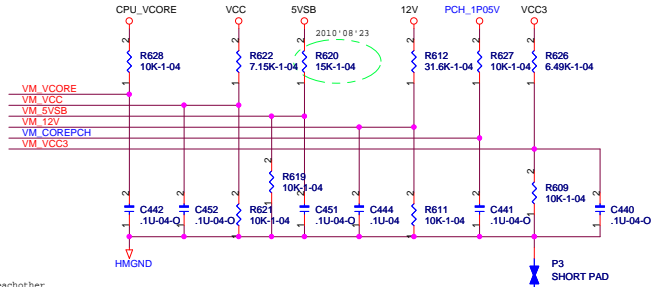
14 SMLK1_SIO_CLK
14 SMLK1_SIO_DATA

SMLK1_SIO_DATA
SMLK1_SIO_CLK

LPT_D7
LPT_D6
LPT_D5
LPT_D4
LPT_D3
LPT_D2
LPT_D1
LPT_D0

LPT_D7_0
LPT_D7_0

10'07'15
del co-lay 8721 circuit



29 COM1_RTS_L
29 COM1_DSR_L
29 COM1_SOUT
29 COM1_SIN
29 COM1_DTR_L
29 COM1_DCD_L
29 COM1_RI_L
29 COM1_CTS_L

VCC3
10K-04
R451
SB_3VSB
VCC3
R450
10K-04
31 SIO_BEEP
GP15
GP64
GP63
FAN_TAC1
FAN_TAC2
FAN_PWM1
FAN_PWM2

VCC3
10K-04
R449
SB_3VSB
VCC3
10K-04
R445
10K-04
CIR_TX

10'07'15
del co-lay 8721 circuit

VCC3
10K-04
R445
10K-04
CIR_TX

SB_3VSB
VCC3
10K-04
R445
10K-04
CIR_TX

13.30 SER_IRQ
14.30 LPC_FRAME_L
14.30 LPC_DRQ0_L
14.30 LPC_AD0_3

13 KB_RST_L
13 A20GATE
13 SIO_33M
15 SIO_48M

10'07'15
del co-lay 8721 circuit

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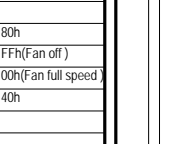
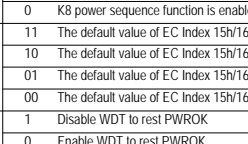
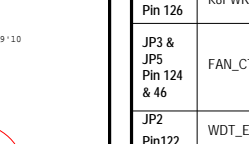
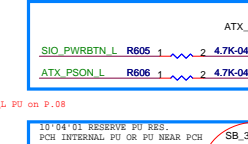
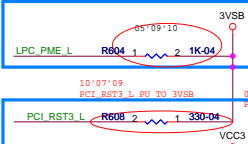
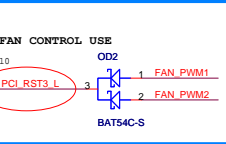
10'07'15
del co-lay 8721 circuit

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del co-lay 8721 circuit

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del co-lay 8721 circuit

10'07'15
del co-lay 8721 circuit

10'07'15
del co-lay 8721 circuit



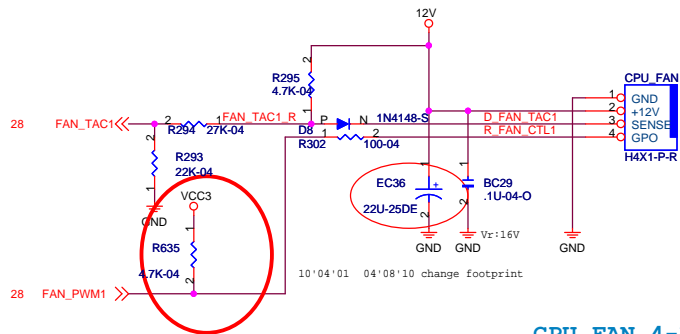
Symbol	value	Description
JP4	1	K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
JP3 & JP5	11	The default value of EC Index 15h/16h/17h is 80h
Pin 124 & 46	10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
JP6	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
Pin 122	00	The default value of EC Index 15h/16h/17h is 40h
JP2	1	Disable WDT to rest PWROK
Pin 122	0	Enable WDT to rest PWROK

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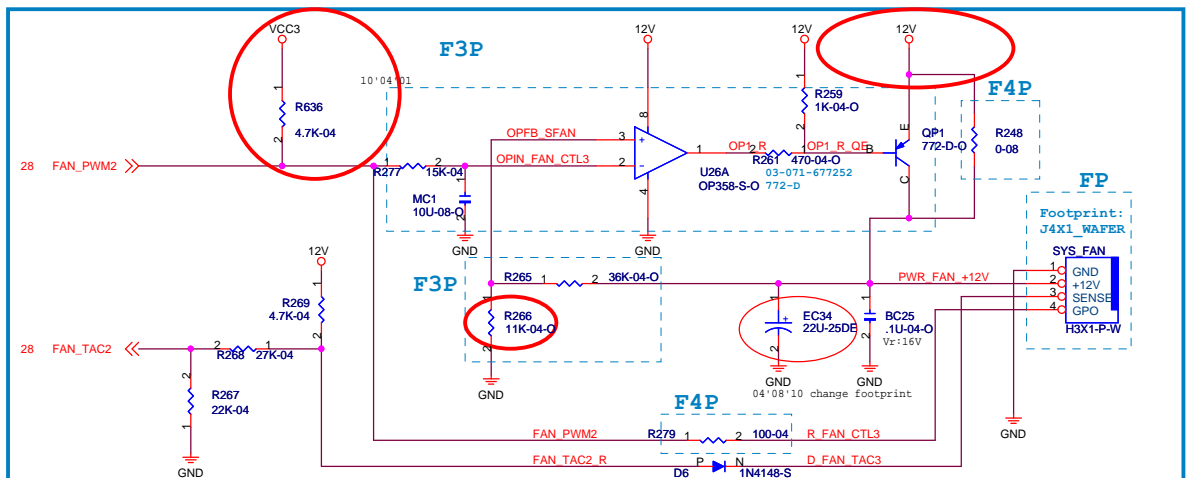
SIO IT8720F

Document Number: 067/ Q65/ H67/ H61 H2-AD

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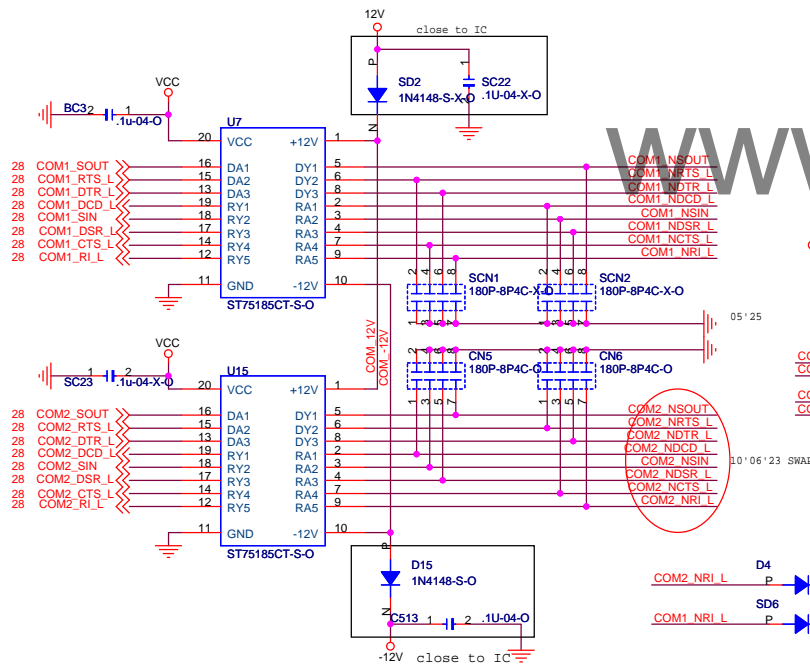


CPU FAN 4-PIN Circuit

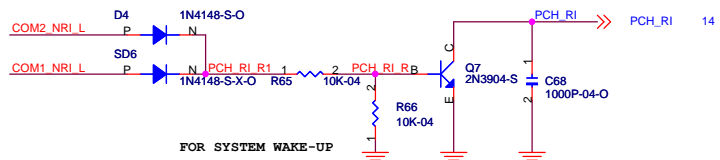
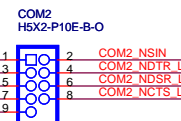
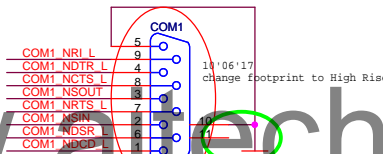


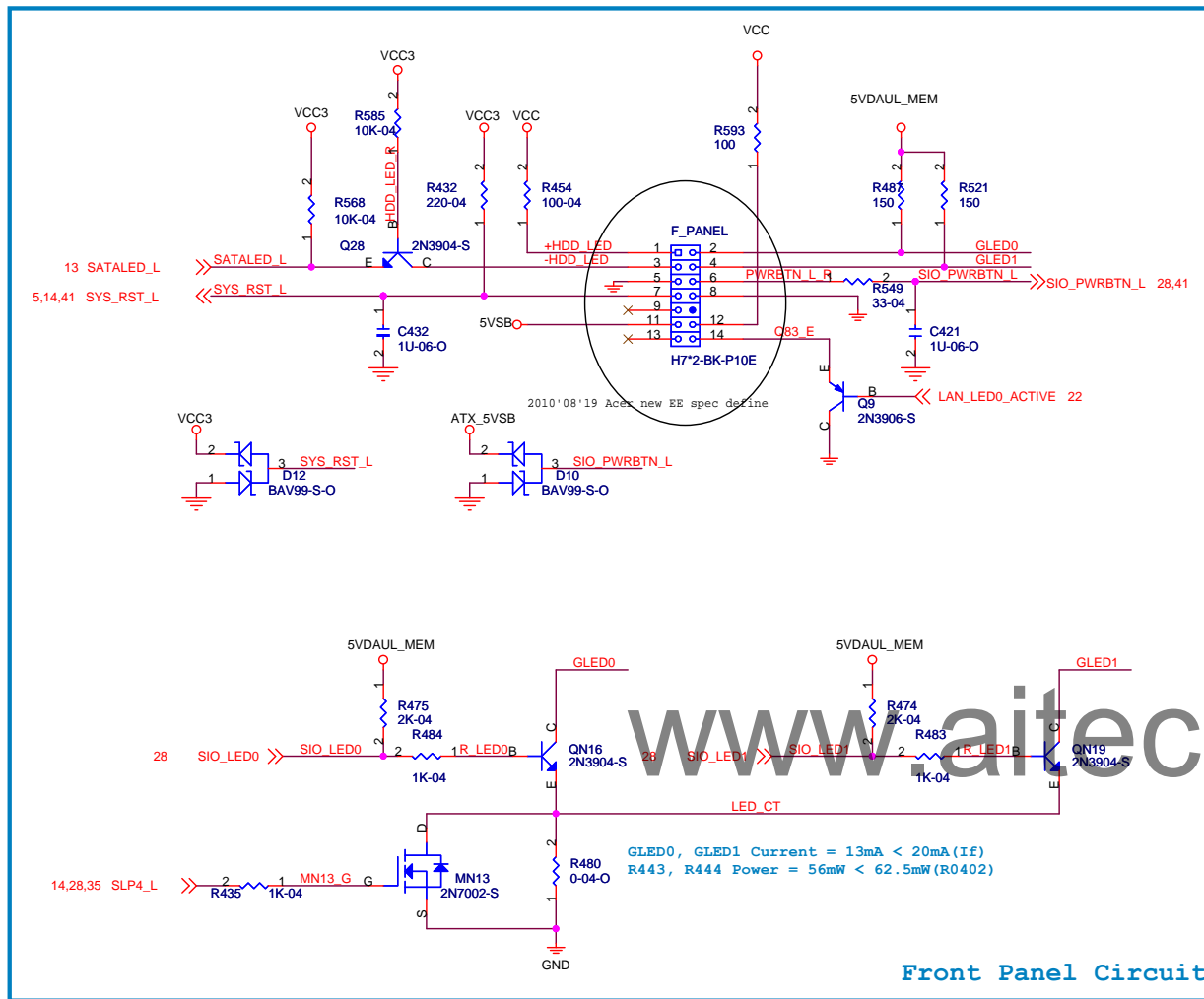
SYS FAN 3-PIN (Co-Lay 4PIN) Circuit

COM PORT I/O



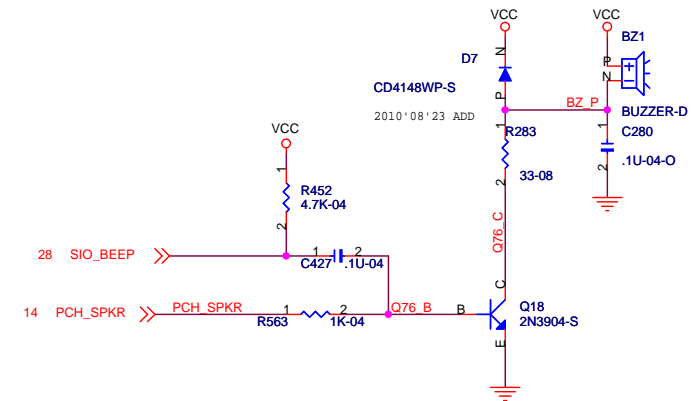
Q67/Q65/H61 (commercial) 上件





Front Panel Circuit

Buzzer Circuit



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Title

F_PANEL, BUZ

Size

Document Number

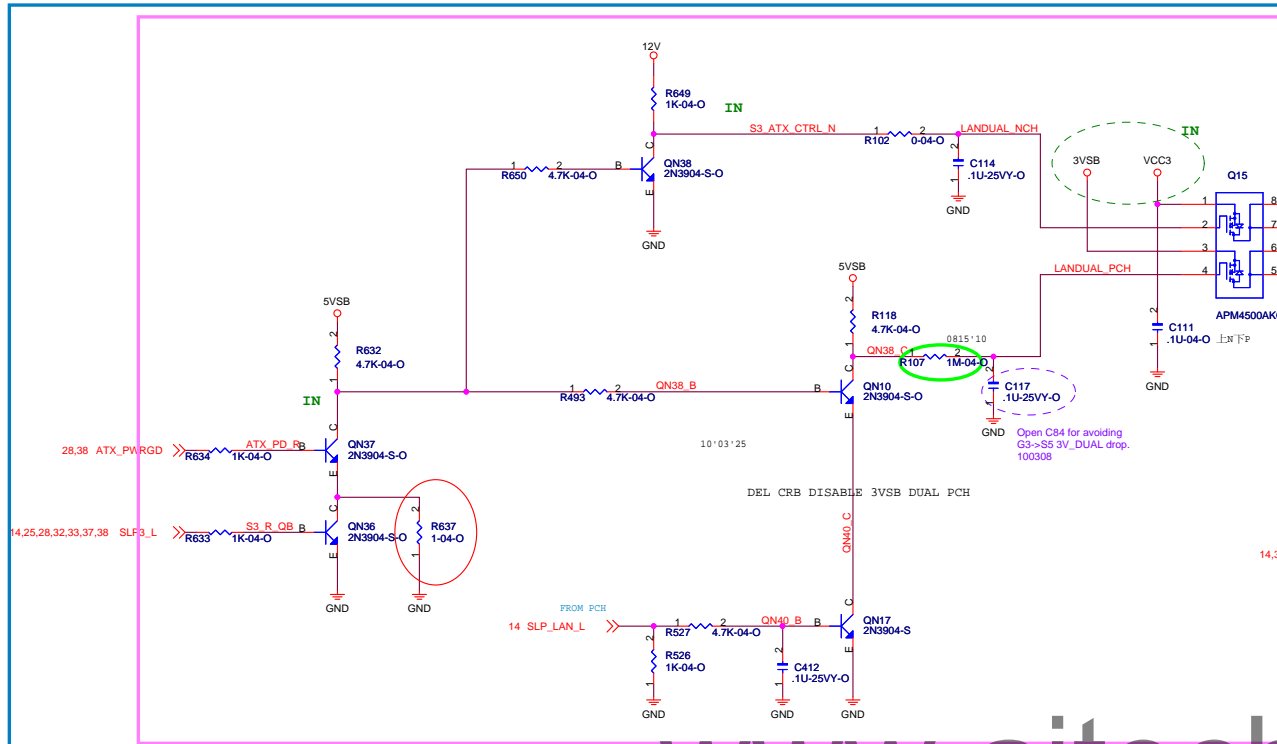
Q67/ Q65/ H67/ H61 H2-AD

Rev

V1.0

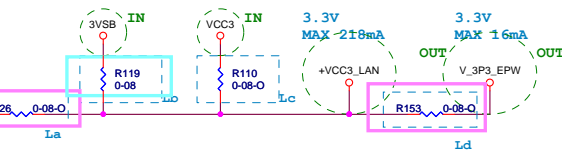
Date: Wednesday, January 12, 2011

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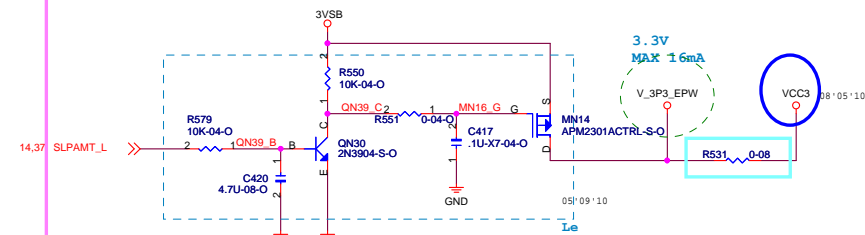


Q67/Q65 上件

H67/H61 (commercial)/H61 (consumer) 上件



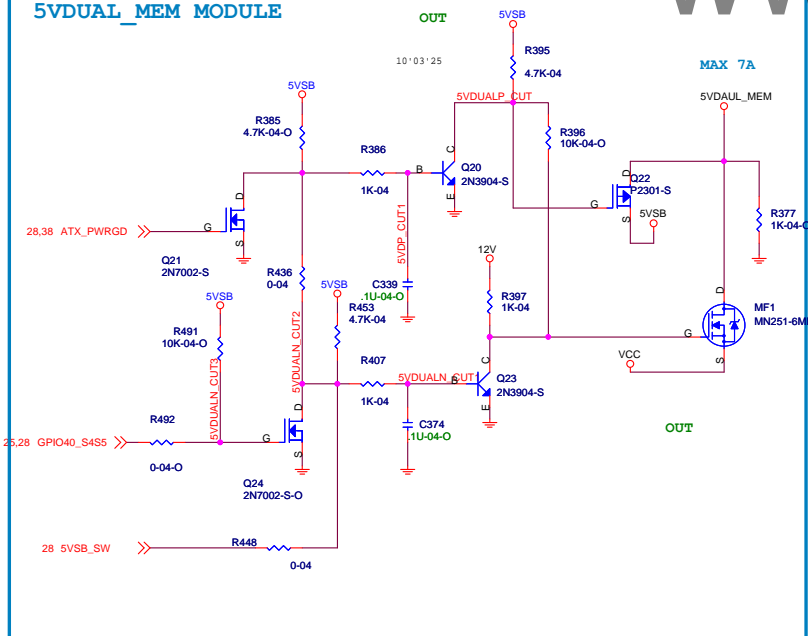
LAN Power Source	La	Lb	Lc
3V LANDUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN(No WoL) or M0 Only	X	X	V



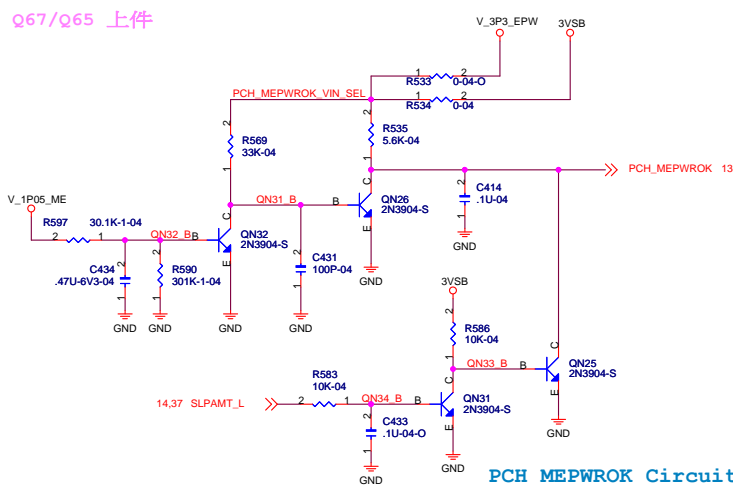
VCC3_EPW control

+VCC3_EPW	Ld	Le
COMBO	V	X
DEFENSIVE	X	V

5VDUAL_MEM MODULE

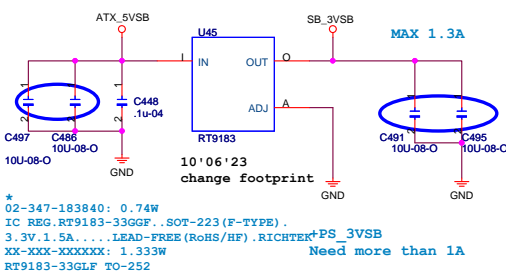


Q67/Q65 上件



PCH_MEPWROK Circuit

3VSB Circuit



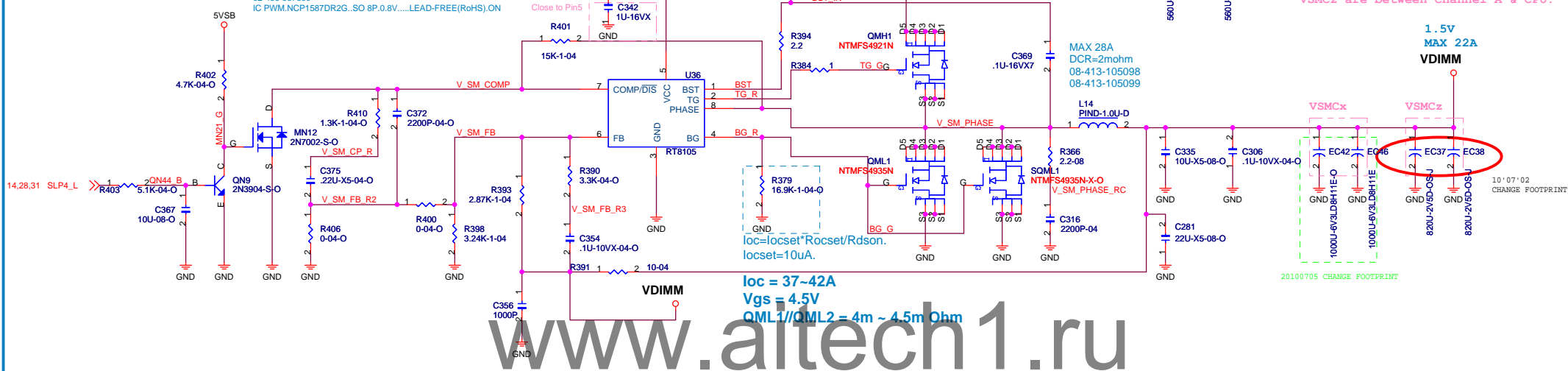
Elitegroup Computer Systems

DC/DC 3VDUAL		
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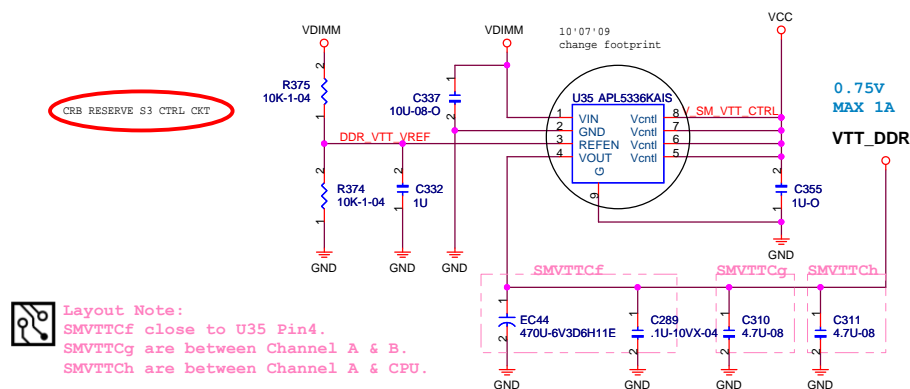
VD IMM

SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-587890
IC PWM.NCP1587DR2G...SO 8P.0.8V.....LEAD-FREE(RoHS).ON

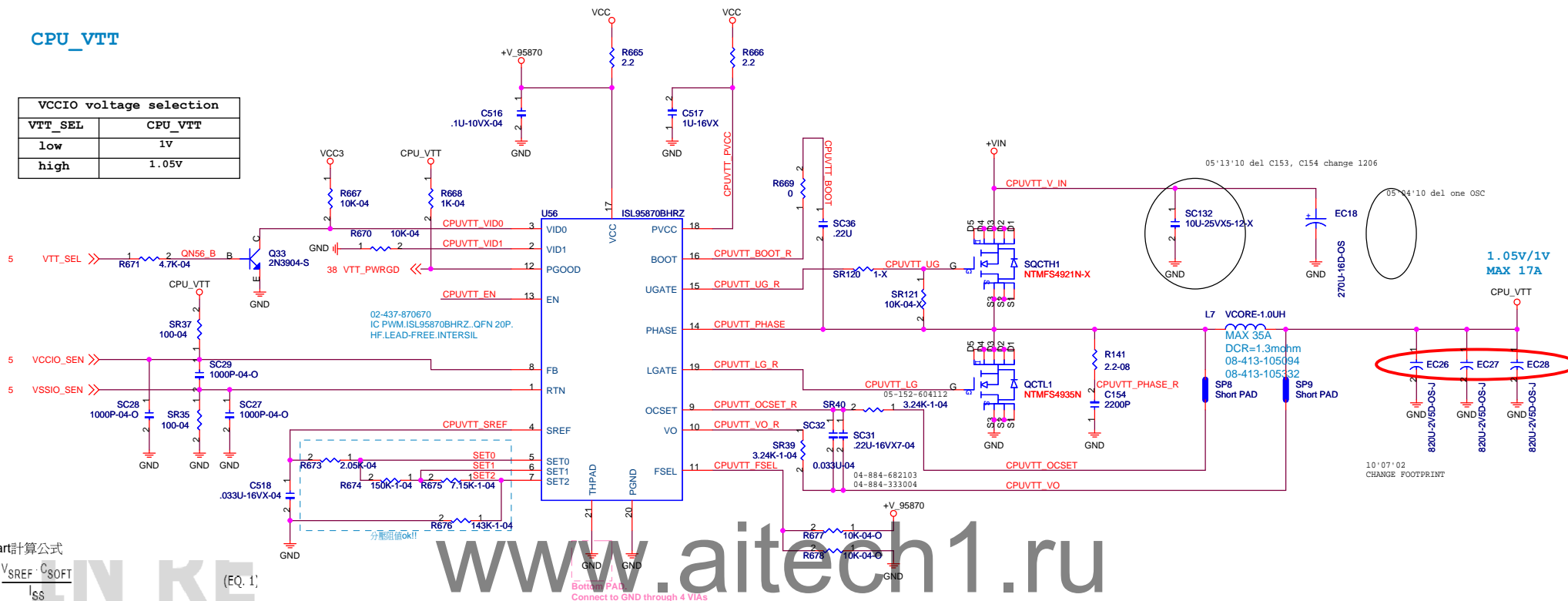


DDR VTT



CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- I_{SS} is the soft-start current source at the 20μA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT			
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}	
1	1	SW0	V_{SET1}	V_{OUT1}	
1	0	SW1	V_{SET2}	V_{OUT2}	
0	1	SW2	V_{SET3}	V_{OUT3}	
0	0	SW3	V_{SET4}	V_{OUT4}	

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (EQ. 21)$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (EQ. 22)$$

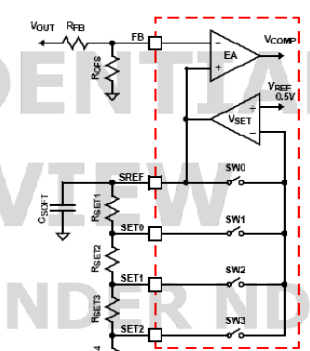
The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}} \right) \quad (EQ. 23)$$

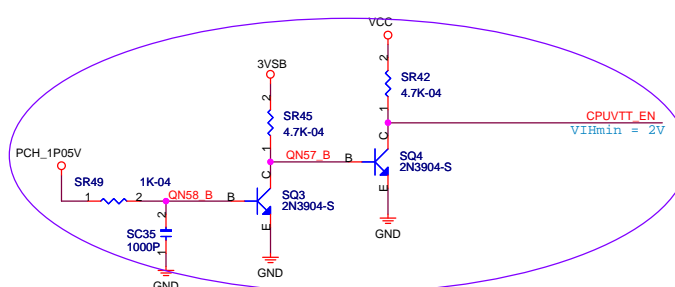
The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (EQ. 24)$$

FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

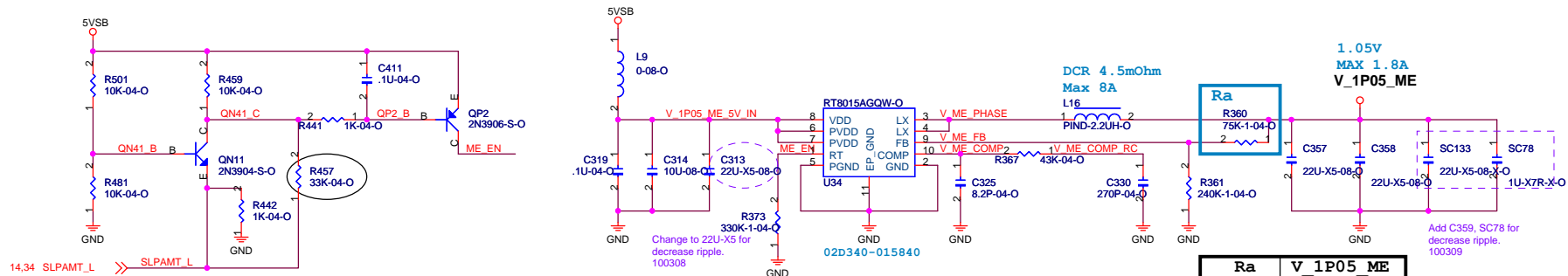


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DC/DC V_CPUVTT

Document Number: Q67/ Q65/ H67/ H61 H2-AD

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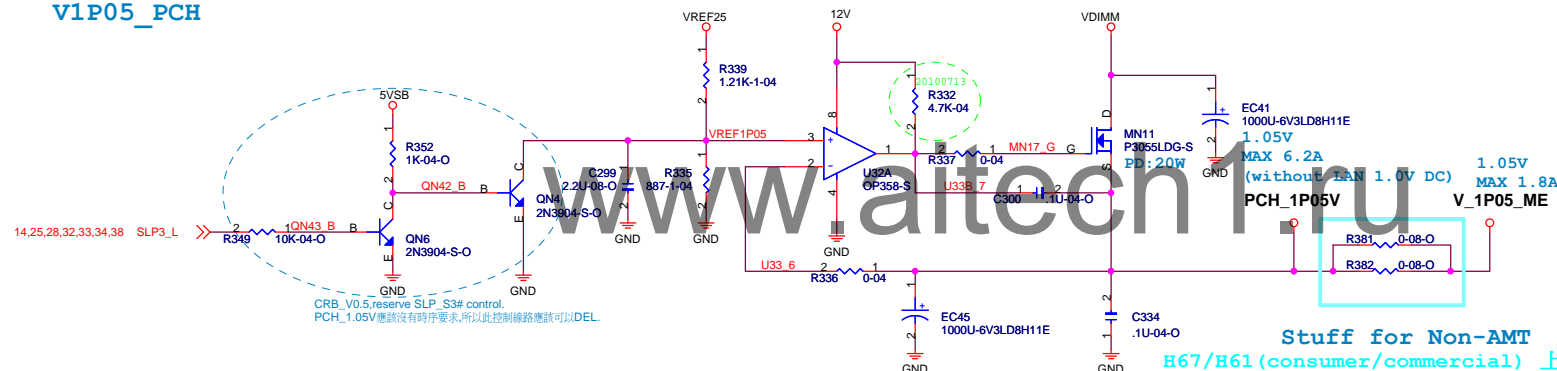


SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable

V1P05_ME

Q67/Q65 上件

V1P05_PCH



BOM Note:

02-340-015840..._dn10_r8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTER

08-413-225094...choke_2r2m_pt4d9x4d6mm
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2*8.2*7.5*6.7
mm.AKL0806MN-2R2M-L3.2....LEAD-FREE(RoHS).MAGIC

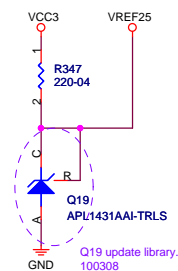
05-152-750113
RES.75K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).

05-152-430103
RES.43K.1/16W.5%.SMD 0402....LEAD-FREE(RoHS/HF).

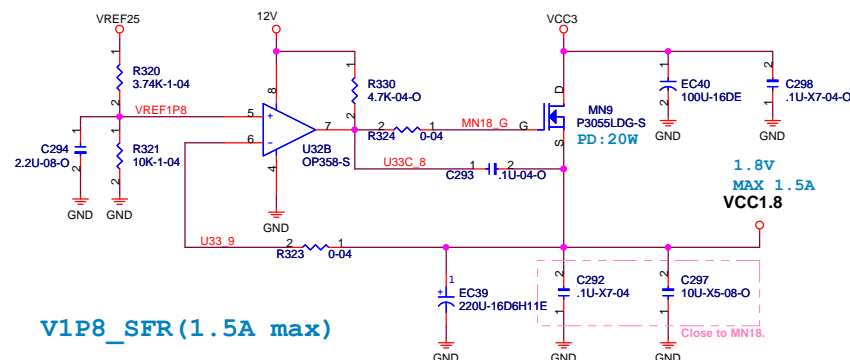
05-152-240114
RES.240K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).

04-880-828100
C/C.8.2pF.50V.0.25pL..NPO...SMD 0402....LEAD-FREE(RoHS/HF).

VREF25



V1P8_SFR (1.5A max)



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Title	DC/DC V1P05_PCH,ME/V1P8_SFR		
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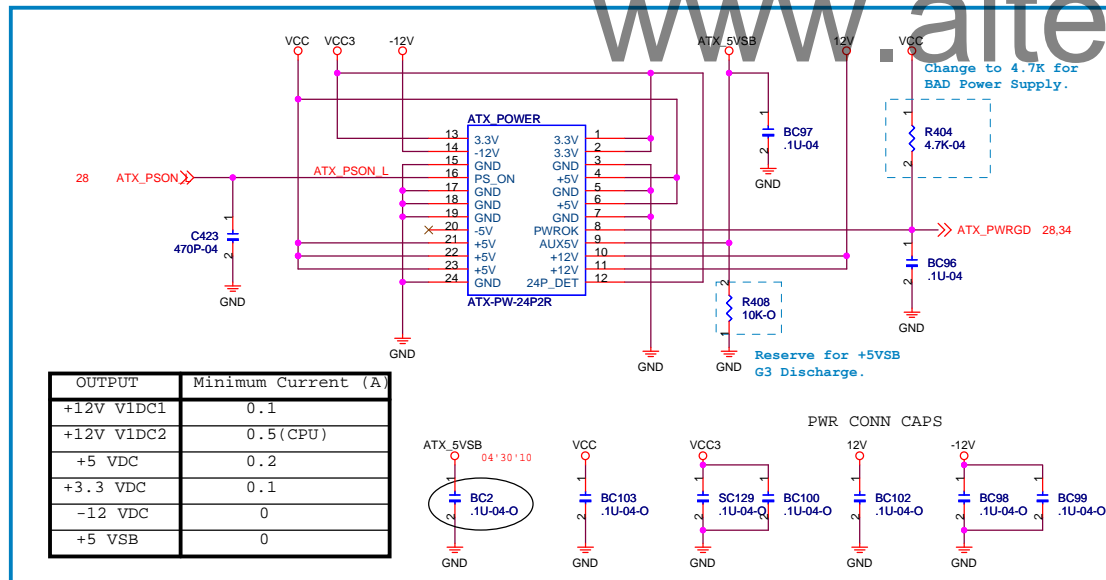
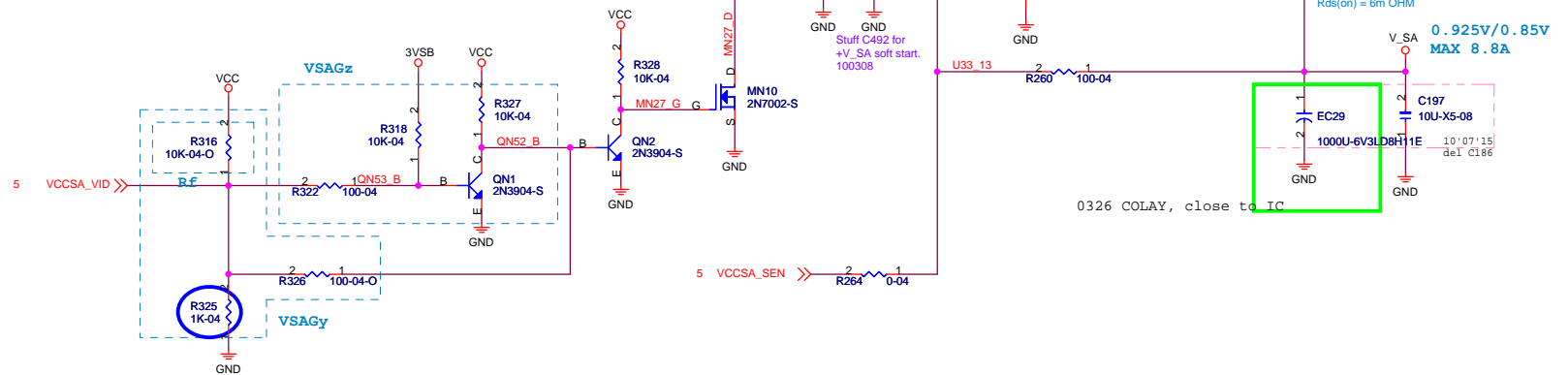
Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

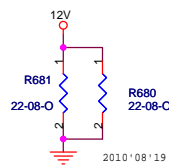
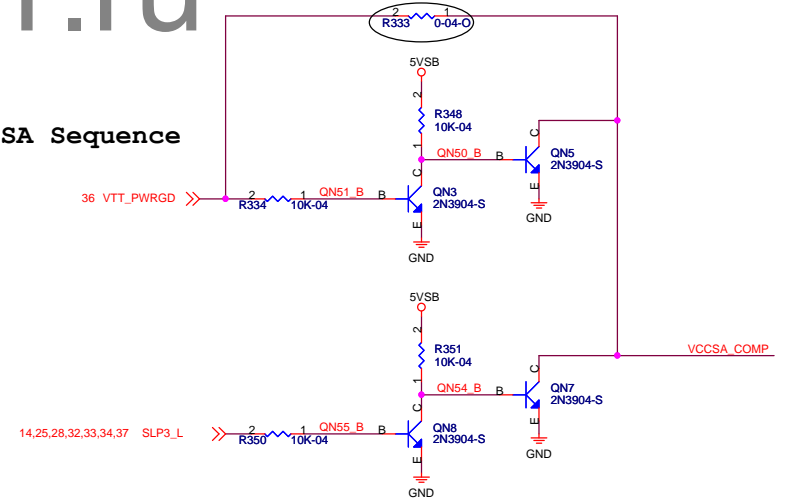
Stuff VSAGy

VCCSA voltage selection	
Rf	+V SA
unstuff	0.85V
stuff	0.925V



ATX Power 24PIN

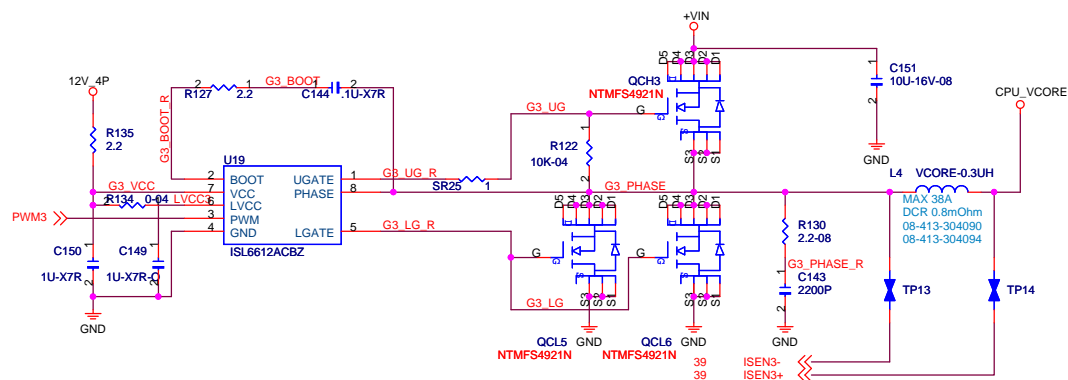
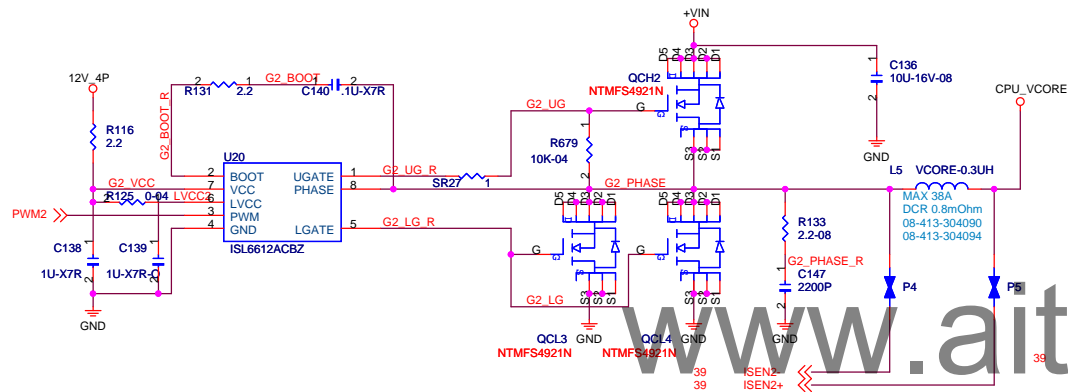
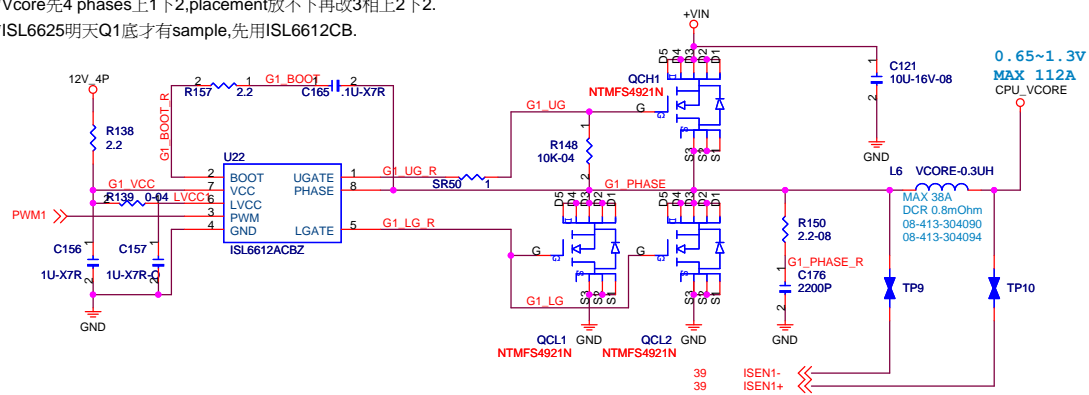
VCCSA Sequence



**Vcore先4 phases上1下2,placement放不下再改3相上2下2.

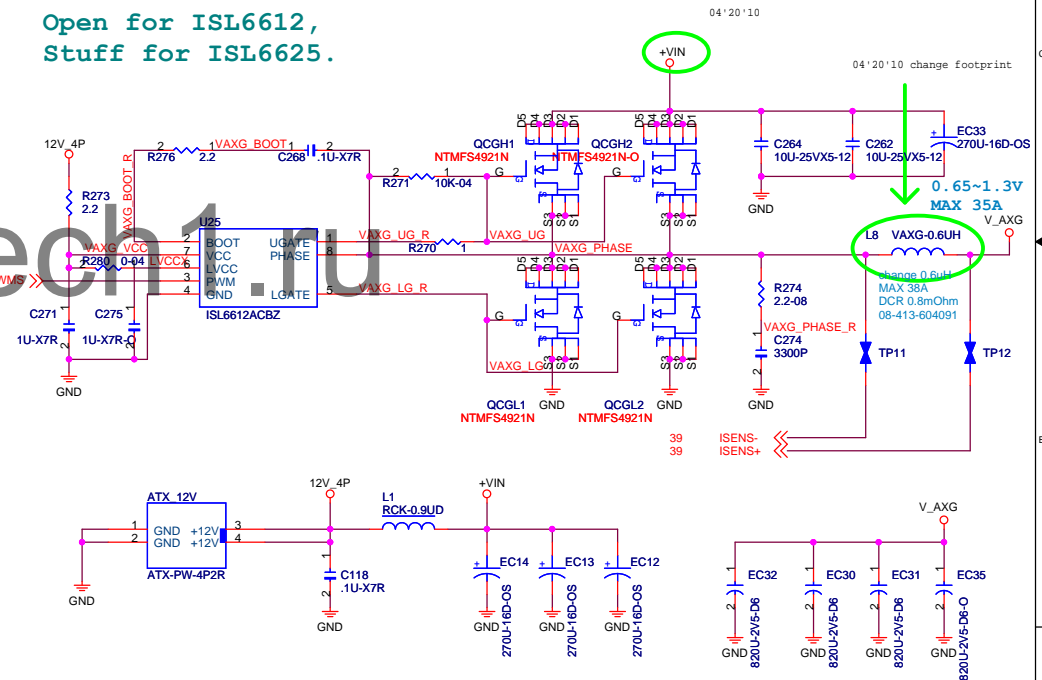
**ISL6625明天Q1底才有sample,先用ISL6612CB.

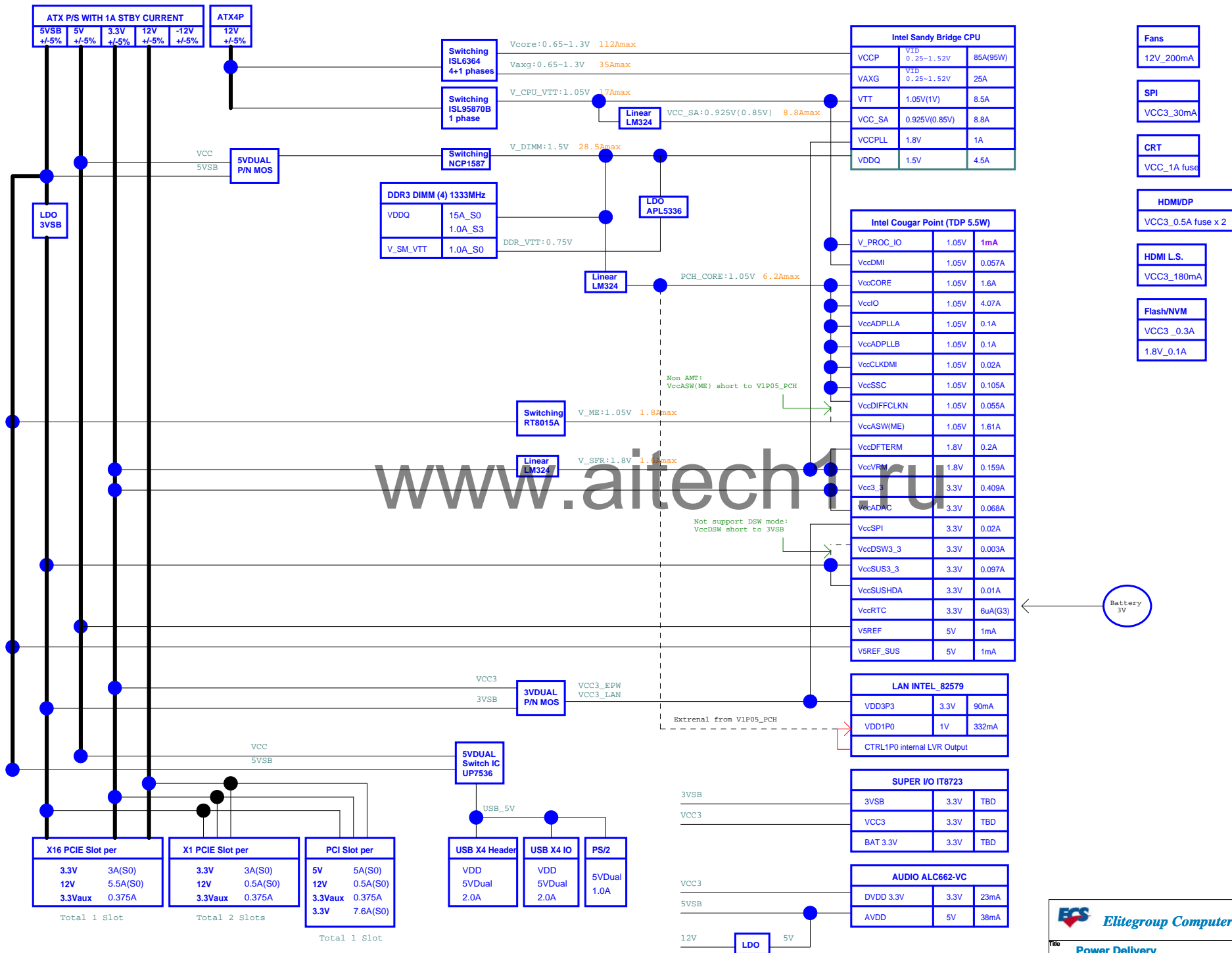
02-415-612672
IC DRIVER:ISL6612ACBZ..SO 8P,LEAD-FREE,INTERSIL

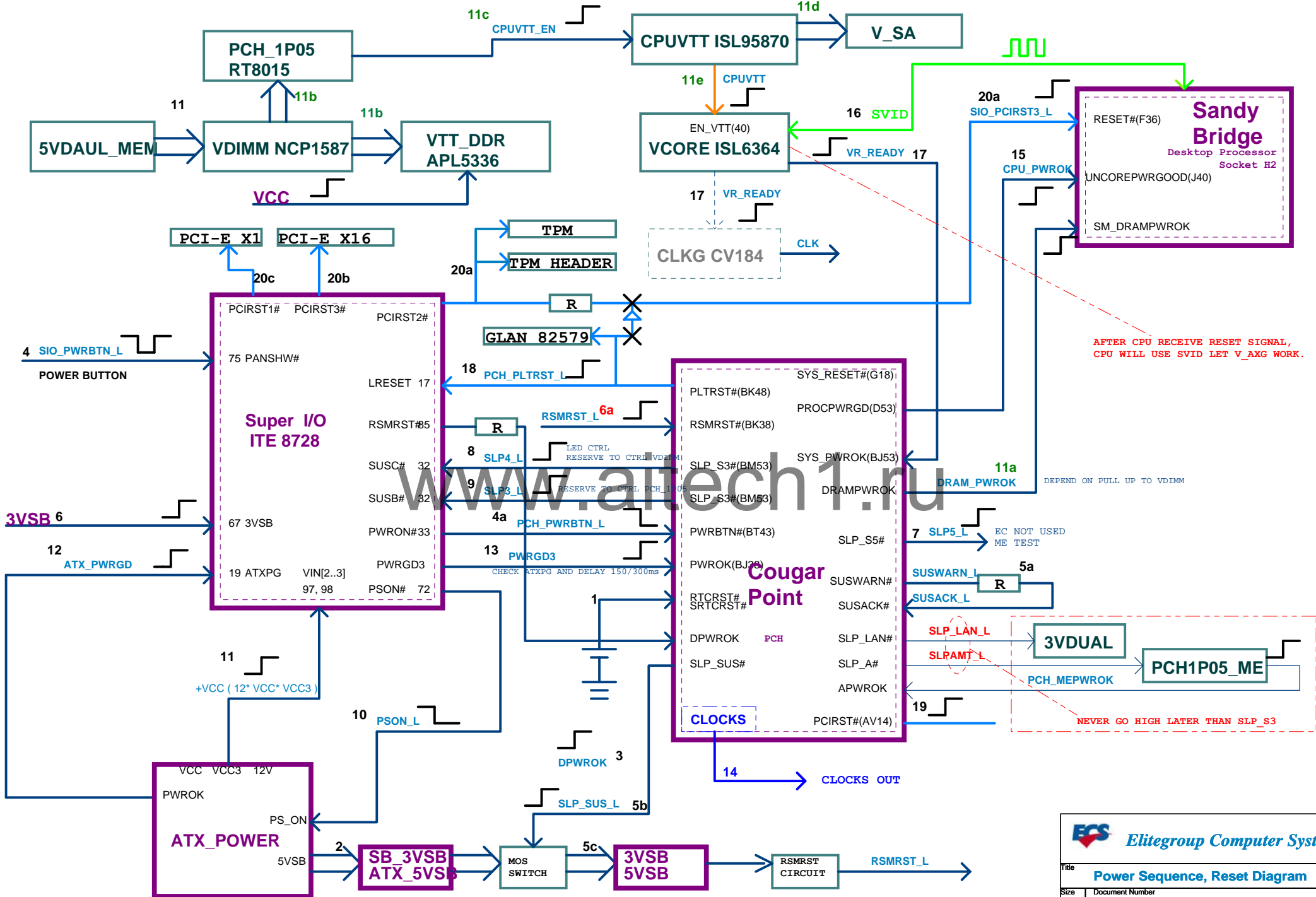


Stuff for ISL6612,
Open for ISL6625.

Open for ISL6612,
Stuff for ISL6625.







NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

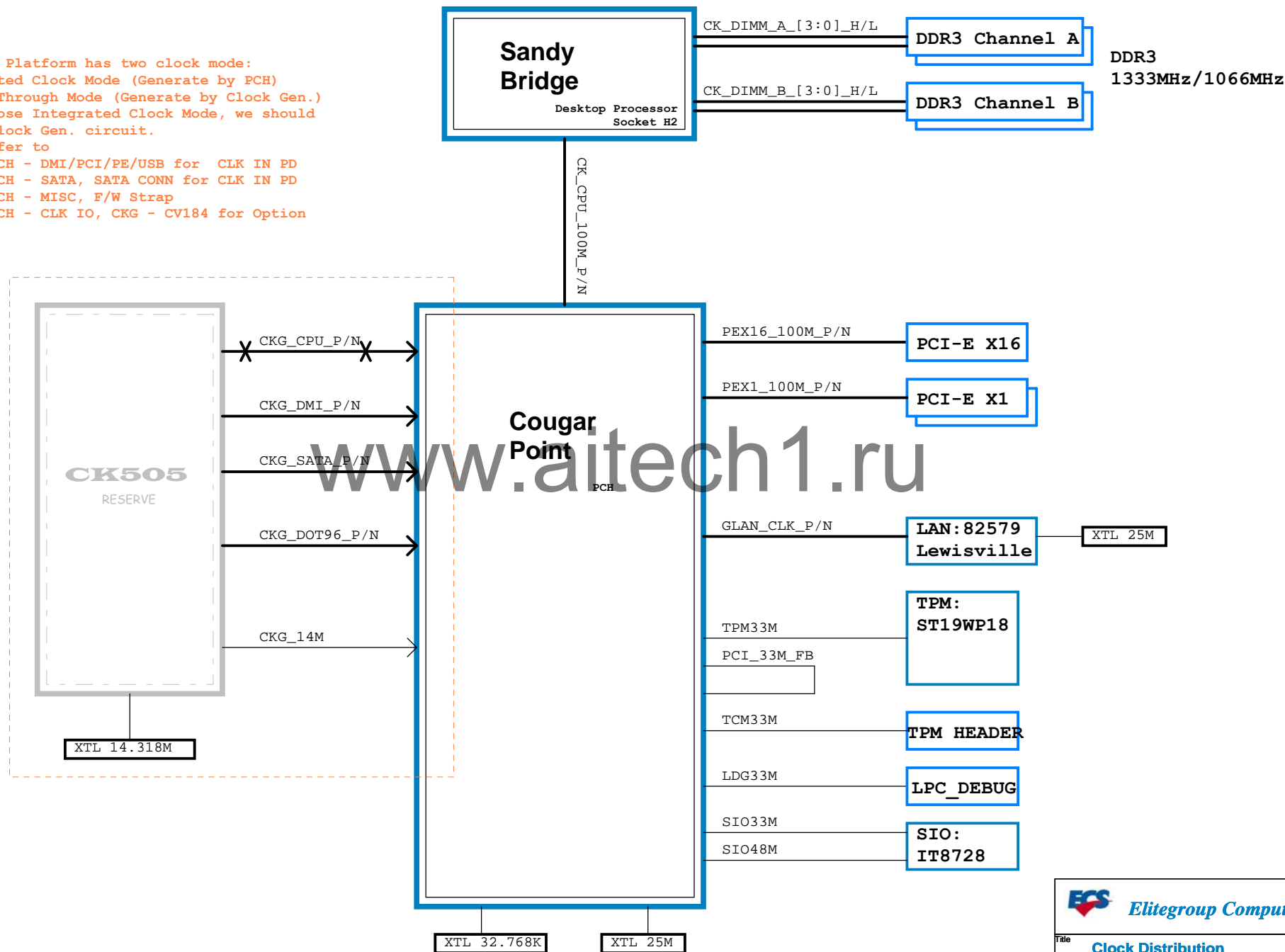
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



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Title
Clock Distribution

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